

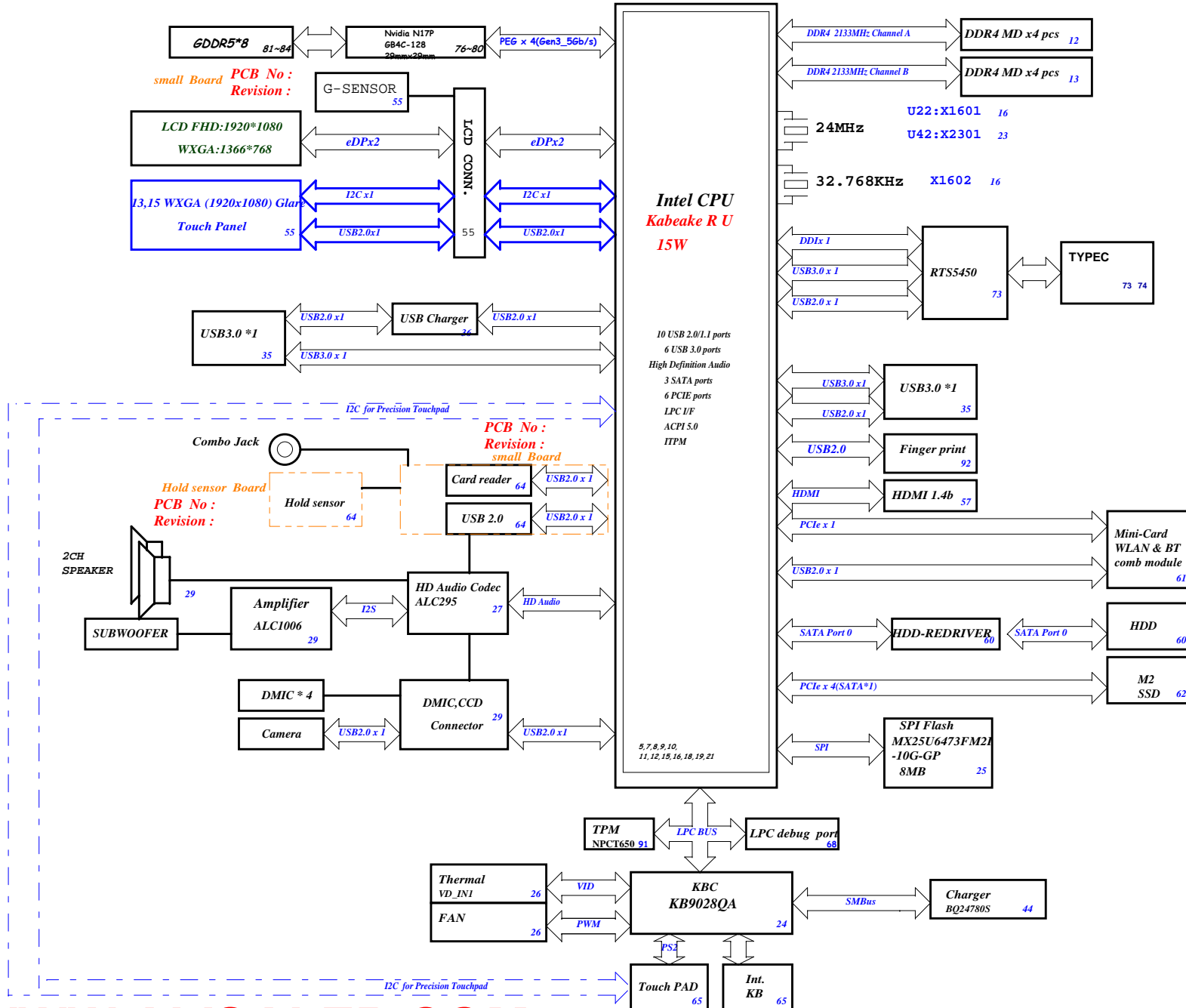
*16932 Buzz\_KBL*  
*Schematics Document*

DY : None Installed  
UMA: UMA only installed  
DIS: DISORTE OPTIMUS installed

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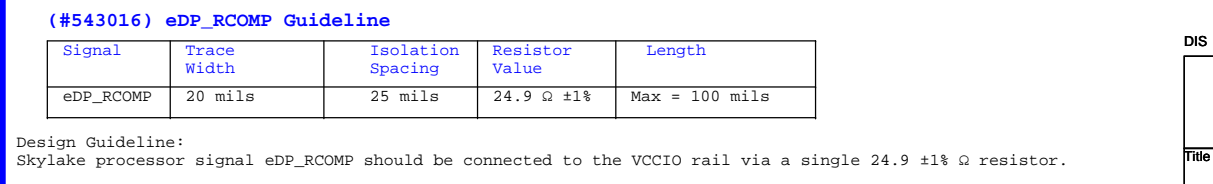
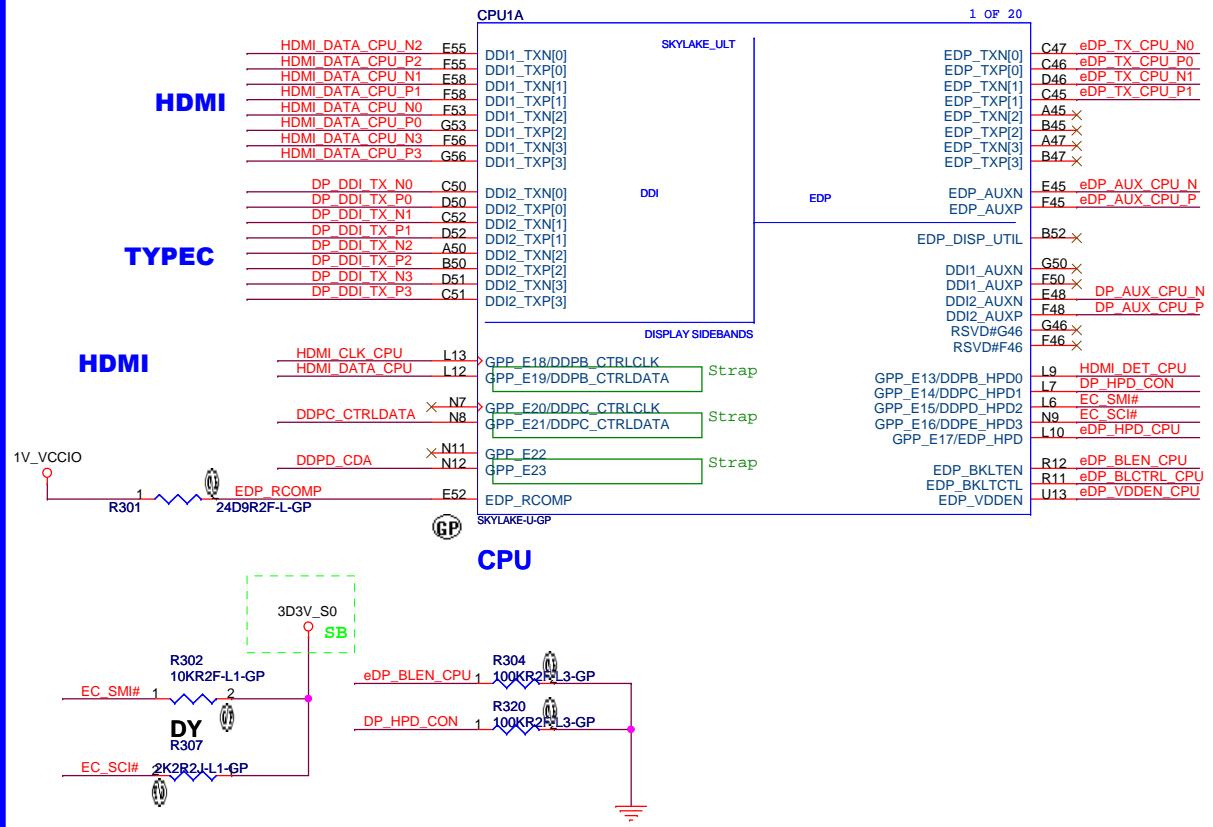
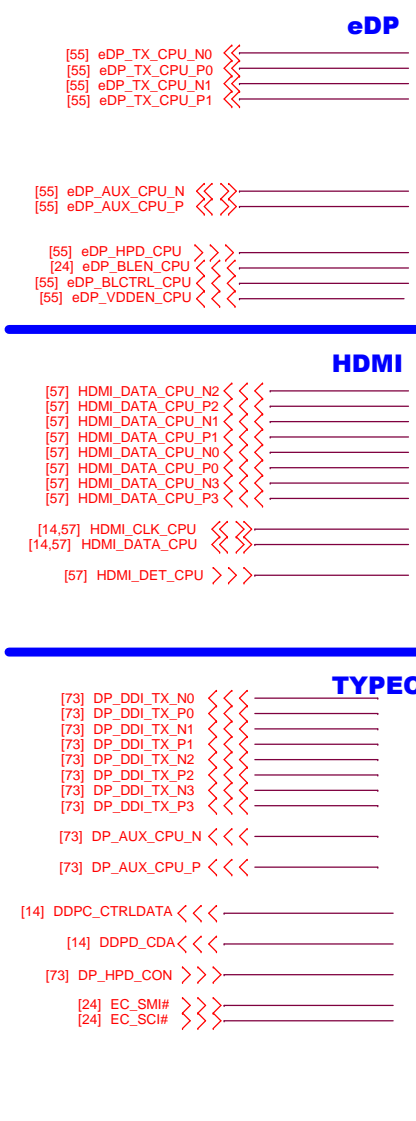
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Project Code: 4PD0CR010001  
PCB No : 16932  
Revision : 2



GPU DC/DC				CHARGER			
RT8813DGQW-GP		85		BQ24780S		44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
5V_S0	1V_VGACORE_S0	AD_5T*	19V_DCBATOUT	5V_S5	1V_VGACORE1_S0	19V_DCBATOUT	3D3V_AUX_S5
GPU DC/DC				SYSTEM DC/DC			
RT8816AGQW-GP		85		RT6228C6QUF-GP		45	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
5V_S5	1V_VGACORE1_S0	19V_DCBATOUT	3D3V_AUX_S5	5V_S5	1D35V_VGA_S0	19V_DCBATOUT	3D3V_S5
GPU DC/DC				SYSTEM DC/DC			
RT8816AGQW-GP		86		RT6228C6QUF-GP		45	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
5V_S5	1D35V_VGA_S0	19V_DCBATOUT	3D3V_S5	5V_S5	1D35V_VGA_S0	19V_DCBATOUT	3D3V_S5
GPU DC/DC				CPU DC/DC			
SY8003ADFC-GP		86		RT3602		46-47	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1D8V_AON_S0	19V_DCBATOUT	1V_CPU_CORE	3D3V_S5	1D8V_AON_S0	19V_DCBATOUT	1V_CPU_CORE
GPU DC/DC				CPU DC/DC			
APE8939GN3-GP		86		AOZ5049		48	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D8V_AON_S0	1D8V_VGA_S0	19V_DCBATOUT	1V_VCC6T	1D8V_AON_S0	1D8V_VGA_S0	19V_DCBATOUT	1V_VCC6T
GPU DC/DC				CPU DC/DC			
APE8939GN3-GP		86		RT9610B		50	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D0V_S5	1V_1D05V_VGA_S0	5V_S5	1V_VCCSA	1D0V_S5	1V_1D05V_VGA_S0	5V_S5	1V_VCCSA
GPU DC/DC				CPU DC/DC			
RT8068A		88		G5388K11U-GP		51	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1V_1D05V_VGA_S0	5V_S5	PWR_VDDQ	3D3V_S5	1V_1D05V_VGA_S0	5V_S5	PWR_VDDQ
CPU DC/DC				CPU DC/DC			
TPS22976DPUR		88		APL5930KAI		51	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0	3D3V_AON_S0	5V_S5	3D3V_S0	3D3V_VGA_S0	3D3V_AON_S0	5V_S5
SYSTEM DC/DC				SYSTEM DC/DC			
G5388K11U-GP		52		9661-25ADJ		53	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
5V_S5	1D0V_S5	3D3V_S5	1D8V_S5	5V_S5	1D0V_S5	3D3V_S5	1D8V_S5
SYSTEM Load switch				SYSTEM Load switch			
TPS22976		40		APE8939		40	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1D5V_S0	5V_S0	1D0V_S5	3D3V_S5	1D5V_S0	5V_S0	1D0V_S5
1D0V_S5	1V_VCCST	1D8V_S5	1D8V_S0	1D0V_S5	1V_VCCST	1D8V_S5	1D8V_S0
SYSTEM Load switch				SYSTEM Load switch			
APE8939		40		APE8939		40	
INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D0V_S5	1V_VCCIO	1D0V_S5	1V_VCCIO	1D0V_S5	1V_VCCIO	1D0V_S5	1V_VCCIO

Main Func = CPU



DIS

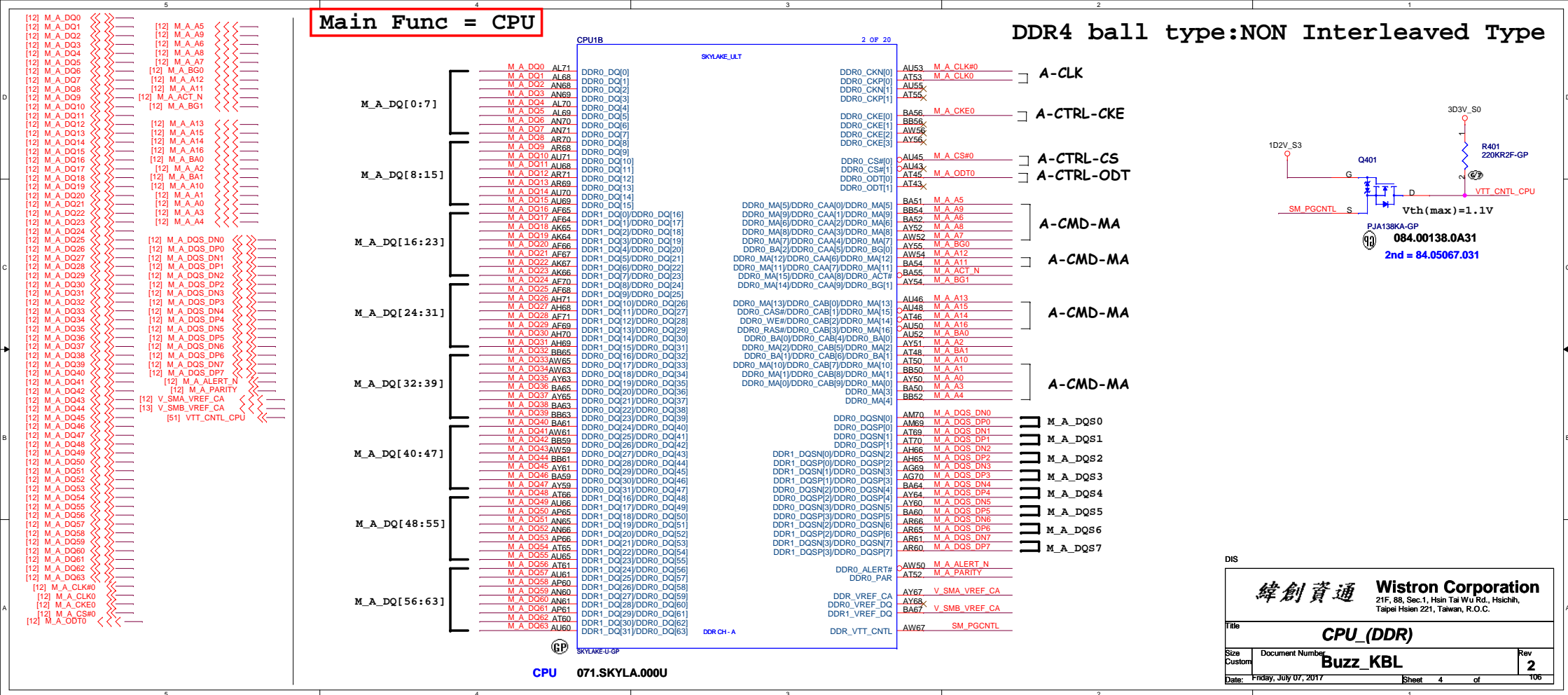
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Title **CPU\_(DISPLAY)**

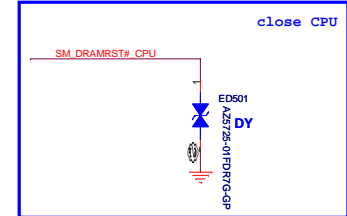
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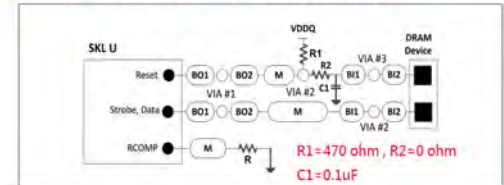
**Main Func = CPU**



```
DDR4 ball type:NON Interleaved Type
```



**Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology Memory Down Strobe/Data/Reset/RCOMP Signal Topologies**



Design Guideline:  
SM\_RCOMP keep routing length less than 500 mils.

	R501
DDP	121ohm(64.12105.6DL)
SDP	200ohm(64.20005.6DL)

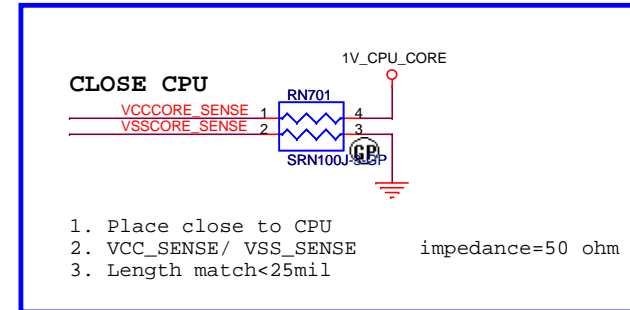
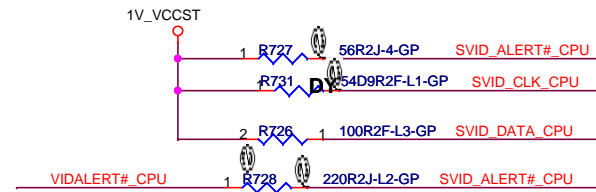
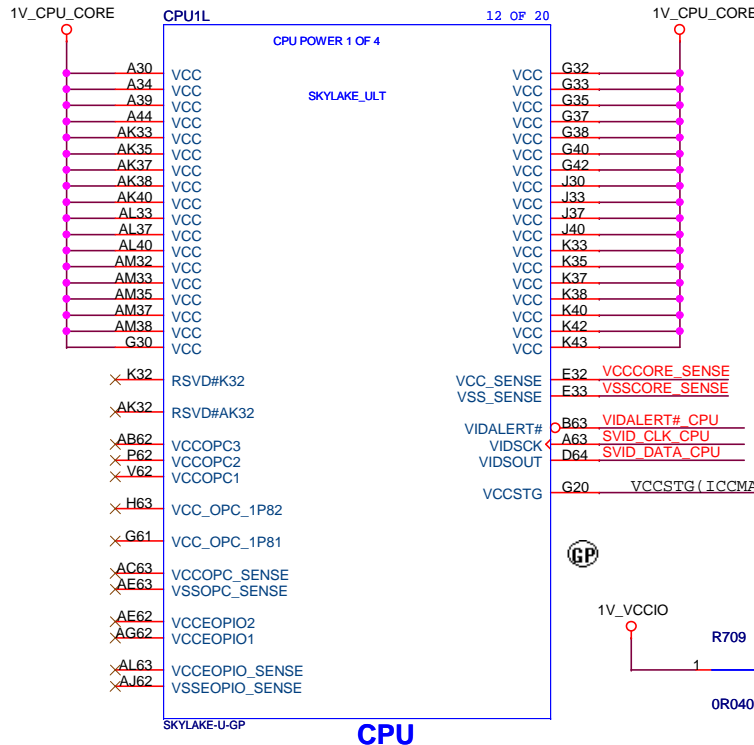
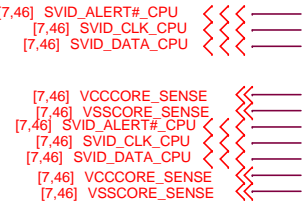
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# Main Func = CPU

## SVID



## Layout Note

1. Place close to
2. VCC\_SENSE/ VSS impedance=50
3. Length match<2

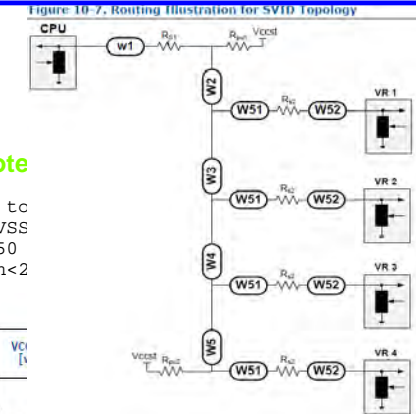


Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R <sub>PU1</sub> [Ω]	R <sub>PU2</sub> [Ω]	R <sub>S1</sub> [Ω]	R <sub>S2</sub> [Ω]	V <sub>CCST</sub> [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R <sub>PU1</sub> [Ω]	R <sub>PU2</sub> [Ω]	R <sub>S1</sub> [Ω]	R <sub>S2</sub> [Ω]	V <sub>CCST</sub> [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

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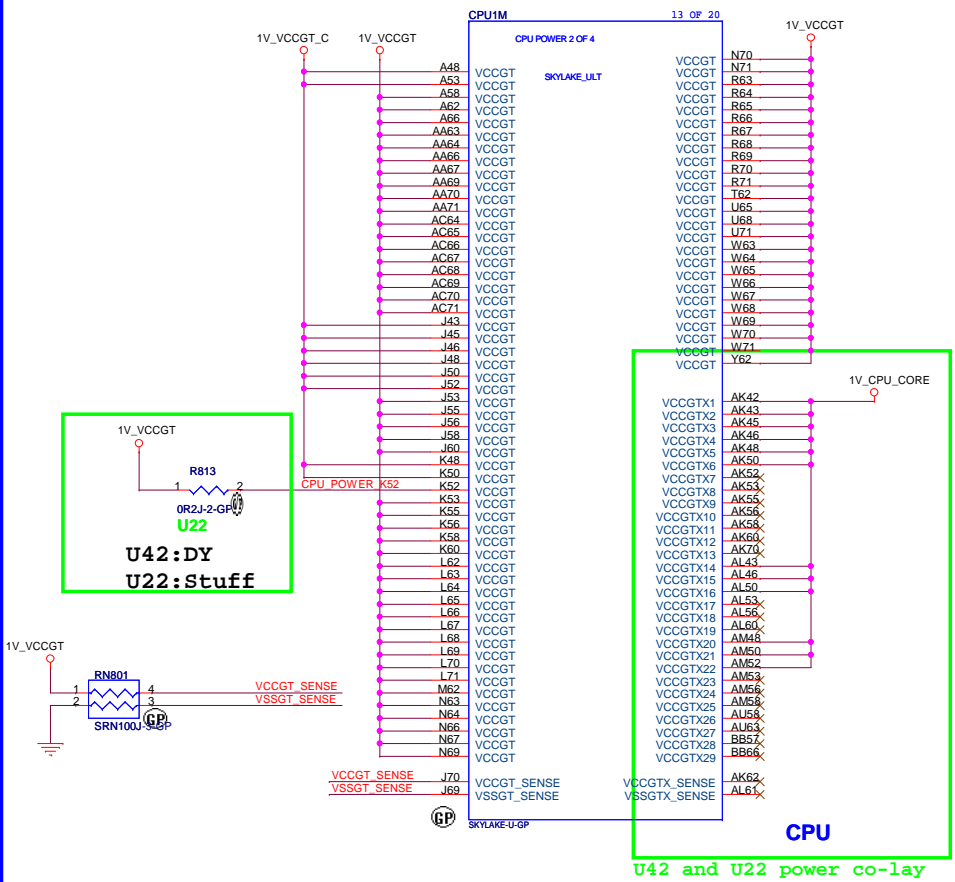
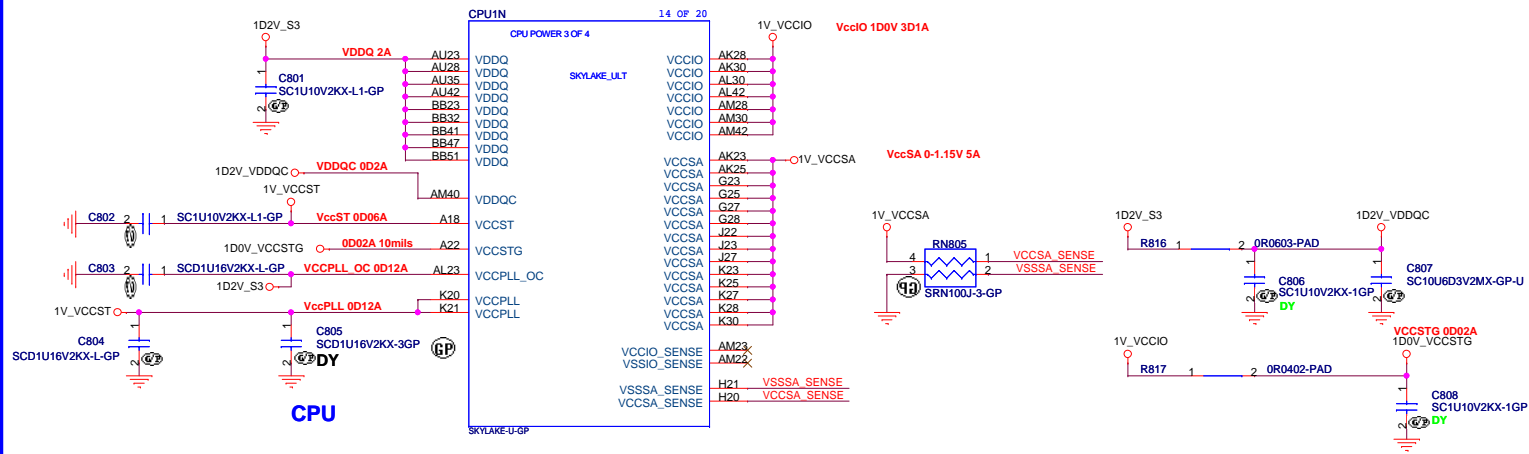
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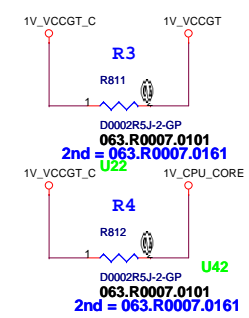
Main Func = CPU

[46] VSSSA\_SENSE  
[46] VCCSA\_SENSE  
[46] VCCGT\_SENSE  
[46] VSSGT\_SENSE



**KBL U42 Board Compatibility with KBL U22/23e**

- 4 Rshunts Required
- R1 – between VCCGTU VR and VCCGTU
- R2 – between VCCGTU and VCCGTU
- R3 – between VCCGT and VCCGT VR
- R4 – between VCCGT and VCCGTU
- Stuff R1 and R3 when U22 or U23e mount on board
- Stuff R2 and R4 and de-pop R1 and R3 when U42 mount on board



R811 R812 Wait change parts

DIS

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# Blanking

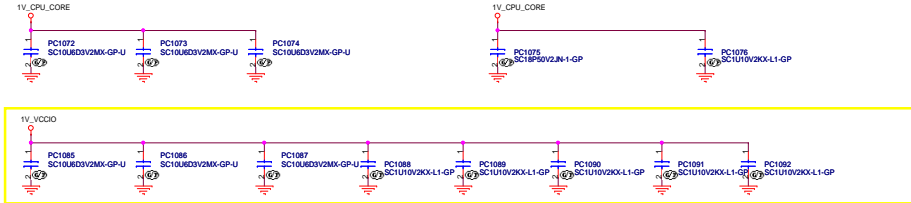
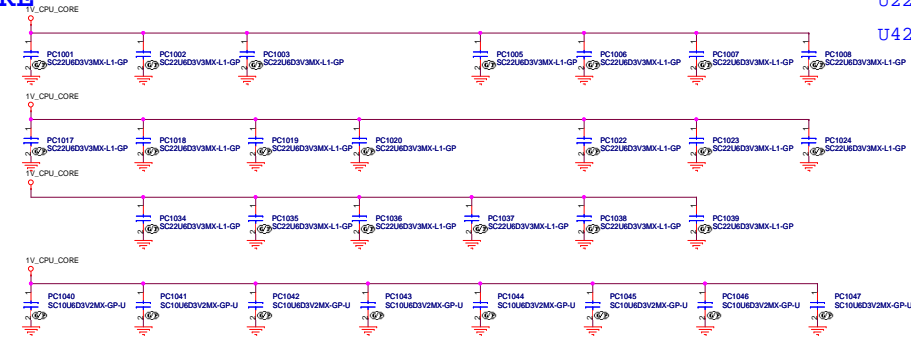
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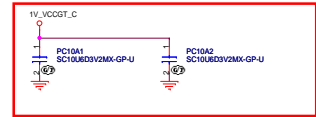
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Size A4	Document Number Buzz_KBL				Rev 2
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Main Func = CPU

VCORE



1V\_VCCIO  
10uF \* 3    1uF \* 4



1V\_CPU\_CORE

U22    0603    22uF \*23    ,    0402    10uF\*20  
U42    0603    22uF \*4    ,    0402    10uF\*20

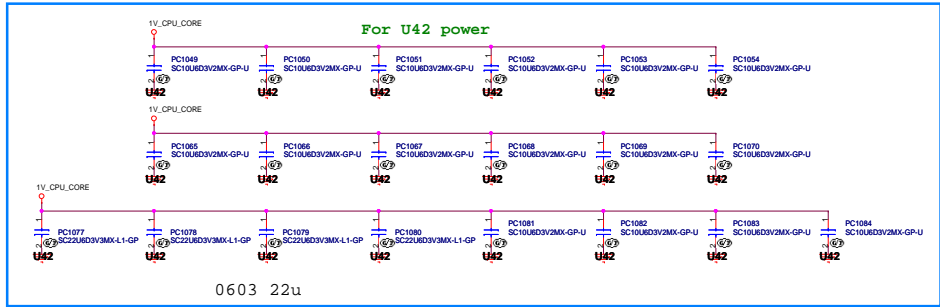
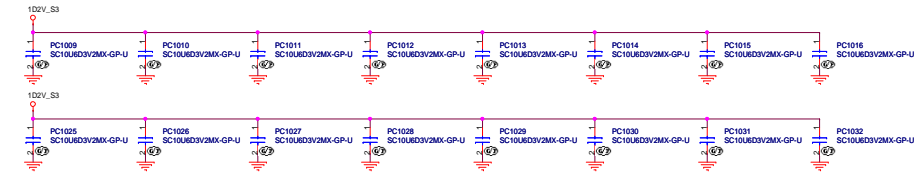


Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
V <sub>CCA</sub>	7x 10 uF 0402 7x 1 uF 0402 or 0201		Place on secondary side, underneath the package
V <sub>CCD</sub>		6x 10 uF 0402	Place as close to the package as possible
V <sub>DDQ</sub>		4x 1 uF 0402	Place as close to the package as possible
V <sub>DDQ</sub>		4x 10 uF 0402	Place as close to the package as possible
V <sub>DDQ</sub>		3 x 22 uF 0603	Place as close to the package as possible
V <sub>DDQ</sub>		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQ pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example shown in Figure 48-3. The 0402 cap to VDDQ. BGA routing should not exceed 48mm (48in). RVP design uses trace L=450mil, W=1mm between BGA and cap. Additional trace routing implemented in RVP design was not required.
V <sub>CCLL</sub>		1x 1 uF 0402	Place as close to the package as possible.
V <sub>CCLL</sub> _DC		1x 1 uF 0201	Do not route V <sub>CCLL</sub> , V <sub>CCLL</sub> _DC, V <sub>CC</sub> closest adjacent layer over any power net other than ground.
V <sub>CC</sub>		1x 1 uF 0402	For VcST: Refer to Figure 48-2 for additional routing details for VcST & VcSTG.

Notes:  
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR.  
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps > Power source.  
3. Due to the difference between the package designs, KBL U 2+2 design requires more on-board decoupling in order to maintain the same leadin.  
4. Diagram of placement for 0402 backside case for CPU decoupling.

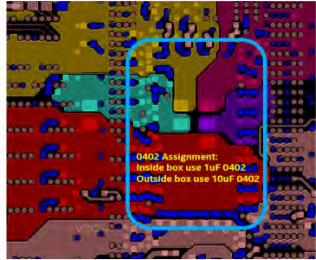


Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
V <sub>CC</sub>	7x 10 uF 0402 31x 1 uF 0402 or 0201		Place on secondary side, underneath the package Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
V <sub>CC</sub> /V <sub>CC</sub> T		9x 22 uF 0603 8x 47 uF 0805 (6.3V) <sup>1</sup> 8x 10 uF 0402	Place as close to the package as possible
V <sub>CC</sub> T	5x 1 uF 0402 or 0201		Place as close to the package as possible
V <sub>CC</sub> T	12x 10 uF 0402 14x 1 uF 0402 or 0201		Place on secondary side, underneath the package
V <sub>CC</sub> T		7x 22 uF 0603 3x 47 uF 0805 (6.3V) <sup>1</sup>	Place as close to the package as possible

Power Layout

48.1.3 Kaby Lake U Compatible Design Recommendation

48.1.3.1 KBL-R U 4+2 / KBL U 2+2 Design Recommendation

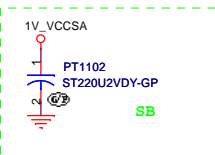
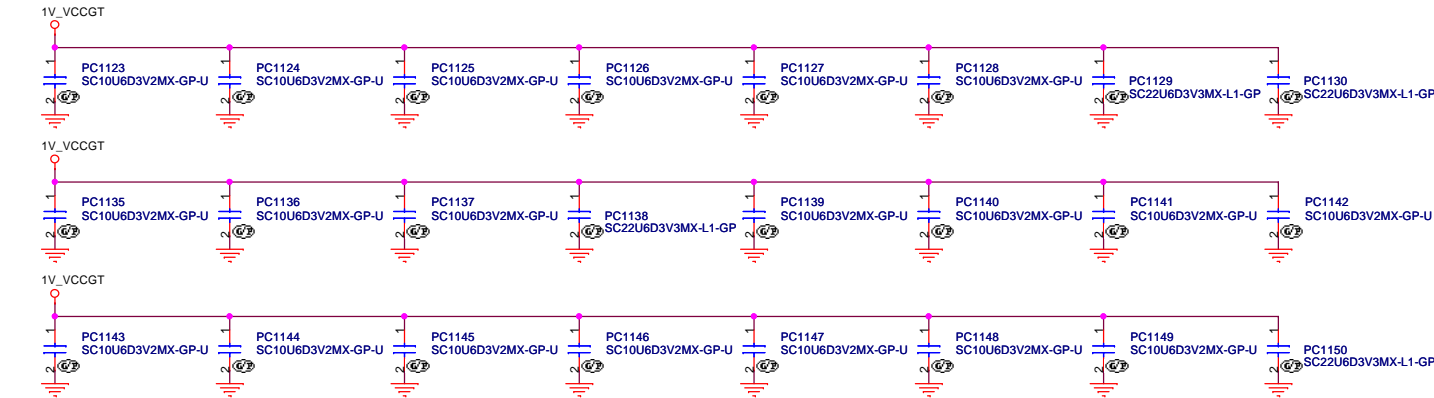
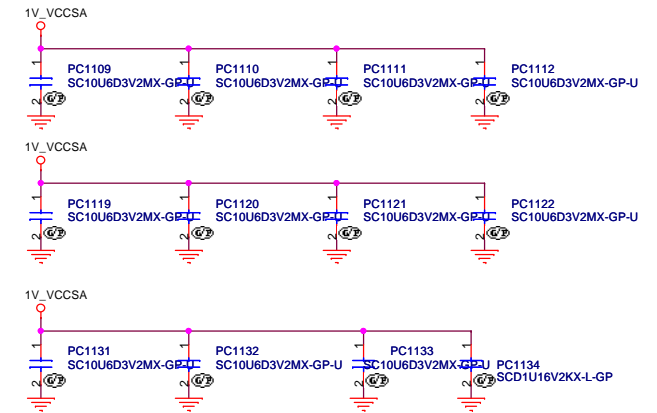
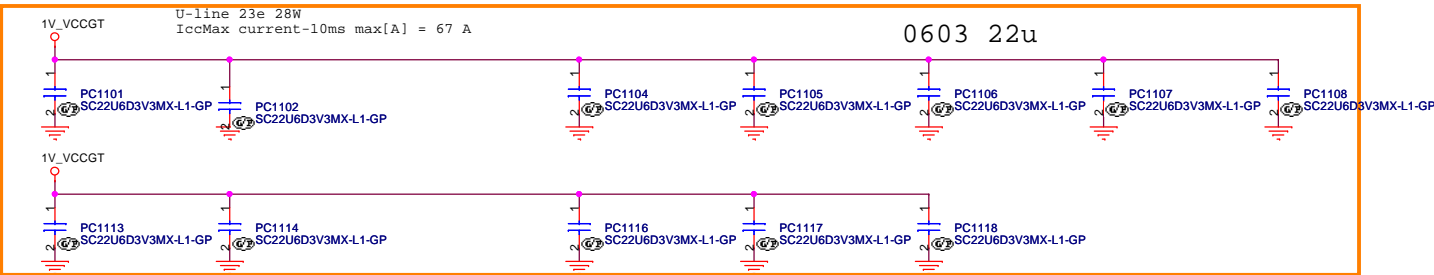
Table 48-3. Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
V <sub>CC</sub> Power Plane at VR output	2x 220 uF (04.5mΩ ESR)	1x 220 uF (04.5mΩ ESR)	Placed at primary side near to VR output
V <sub>CC</sub> Power Plane at VR output	1x 220 uF (04.5mΩ ESR)		Placed at backside side near to VR output
V <sub>DDQ</sub> Power Plane at VR output	2x 220 uF (04.5mΩ ESR)		Placed at primary side near to VR output
V <sub>DDQ</sub> Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
V <sub>DDQ</sub> Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
V <sub>CC</sub> Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
V <sub>CC</sub> Power Plane at VDDA VR output	1x 0.1uF 0402		Placed at primary side near to VR output

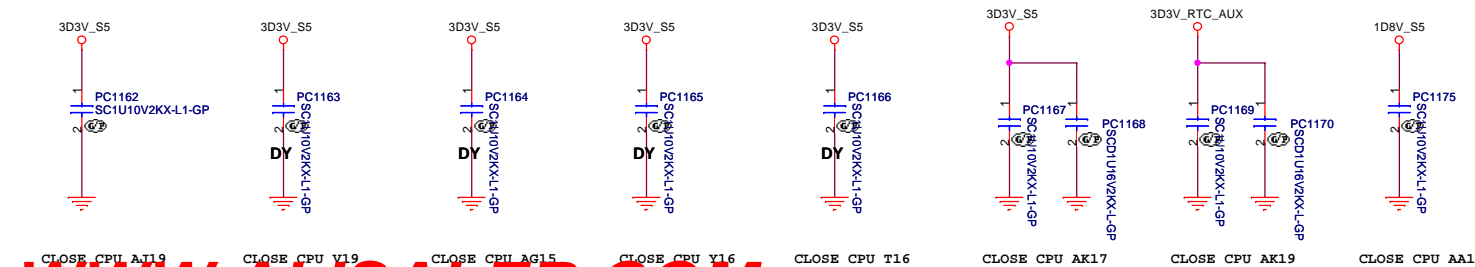
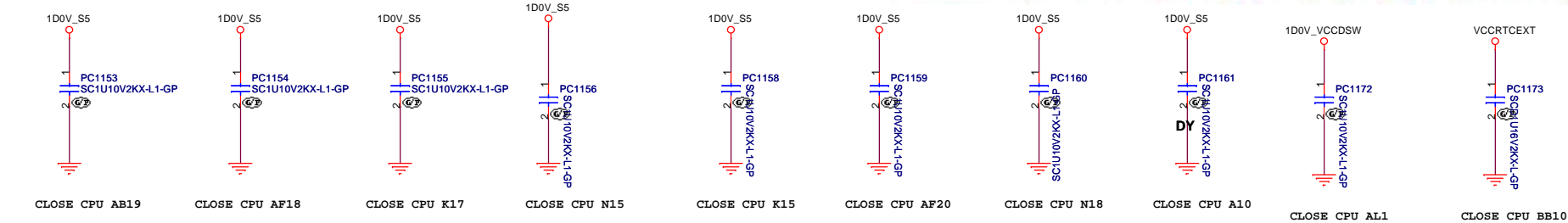
Notes:  
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.  
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Main Func = CPU

## SLICED GT



U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
	GT	750KHz	40A (31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	36x22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF



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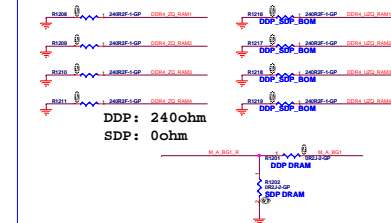
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Title CPU\_(Power CAP2)

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## SSD & DDP SETTING



### DDP x16 and SSD x16 Compatible Layout

Alternate two layout, risk of VSS offset increases a little

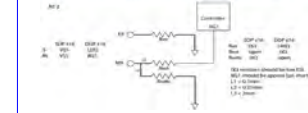
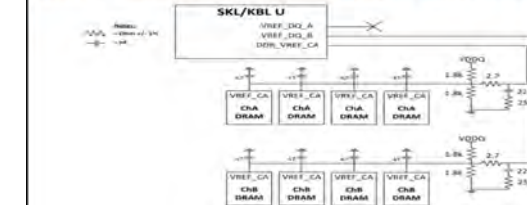
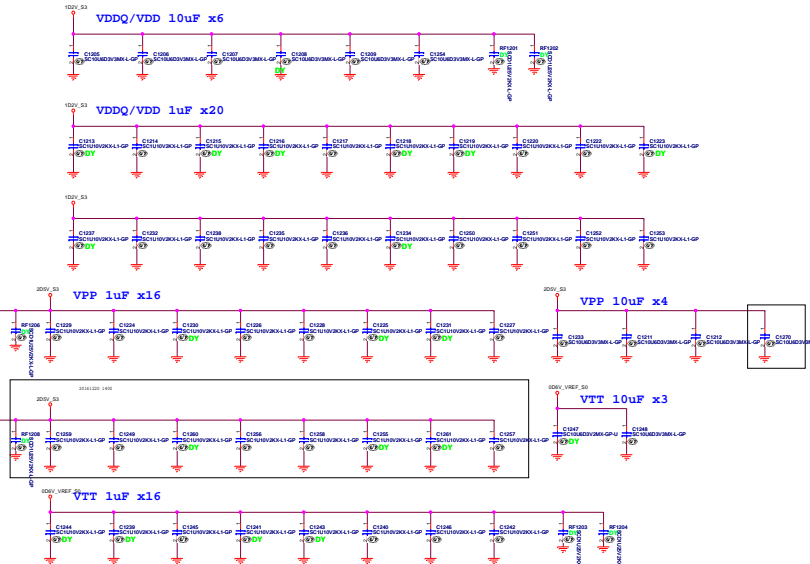


Figure 4-3: SKL/KBL U DDR4 Memory Down VREF-DQ and VREF-CA Overview



### DDR4 On Board RAM Power Decouple Cap

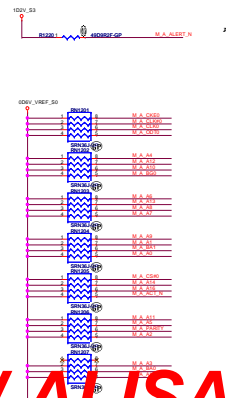


### 4.14.3 KBL-R DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-27: DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x uF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	9 as near each x16 DRAM device as possible	32x 1uF (0402) (All stuffed)	
	VPP	Distributed around the DRAM device	19x 10uF (0603) (All stuffed)	
	VTT	2 as near each x16 DRAM device as possible	16x 1uF (0402)	
	VTT	Distributed around the DRAM devices	5x 10uF (0603)	
			2 as near each x16 DRAM device as possible	
			16x 1uF (0402)	
			4x 10uF (0603)	



DQ80	DQ0-DQ7
DQ81	DQ8-DQ15
DQ82	DQ16-DQ23
DQ83	DQ24-DQ31
DQ84	DQ32-DQ39
DQ85	DQ40-DQ47
DQ86	DQ48-DQ55
DQ87	DQ56-DQ63

please notice that signal B01 (pin#9) and UQ0 (pin#9) are required

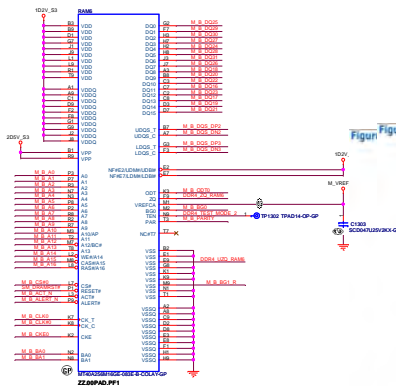
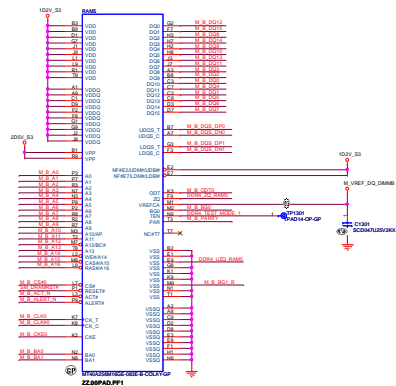
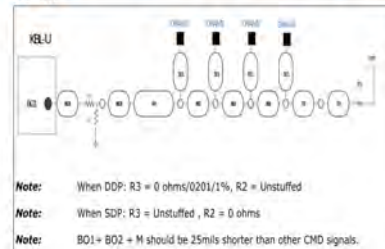
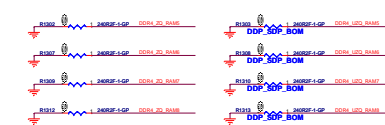


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology



## SDP & DDP SETTING



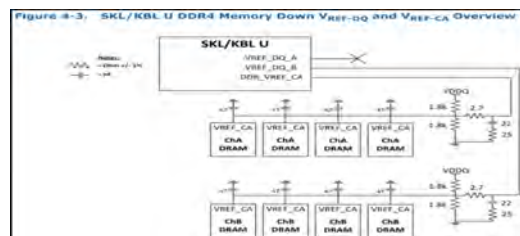
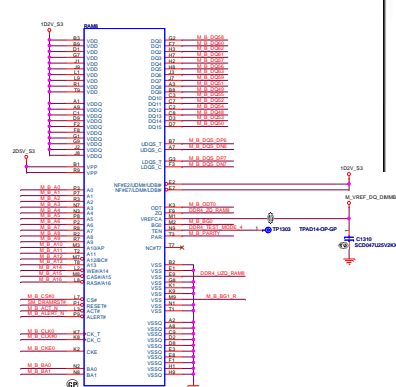
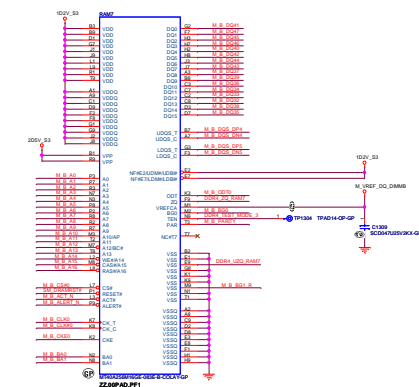
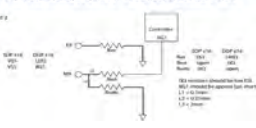
DDP: 240ohm

SDP: 0ohm

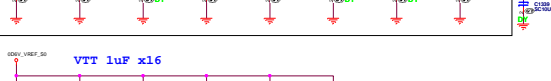
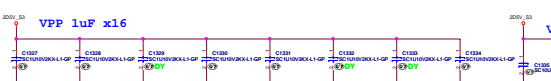
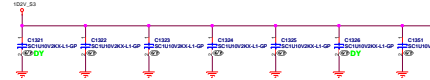
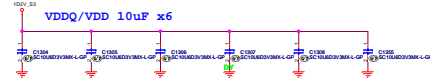


DDP x16 and SDP x16 Compatible Layout

Alternate two layout, risk of VSS offset increases a little



DDR4 On Board RAM Power Decouple Cap

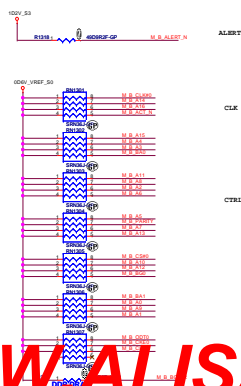


### 4.14.3 KBL-R DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-27. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x $\mu$ F (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1 $\mu$ F (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10 $\mu$ F (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1 $\mu$ F (0402)	
		Distributed around the DRAM devices	5x 10 $\mu$ F (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1 $\mu$ F (0402)	
		Distributed around the DRAM devices	4x 10 $\mu$ F (0603)	





# SSID = STRAP

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confidentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

Name	Internal Pull-up/ Pull Down (Note 1)	De-Bunch (Note 2)	Input	Output	Multiplexed With	Default	RM or SMI Capable	Note
GPP_B22	20K PD (see note)	No	No	No	SPI0_MOSI	GPD	None	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts.
GPP_B23	20K PD (see note)	Yes	No	No	SMI_ALERT# / PCMRST#	GPD	RM SMI	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts.

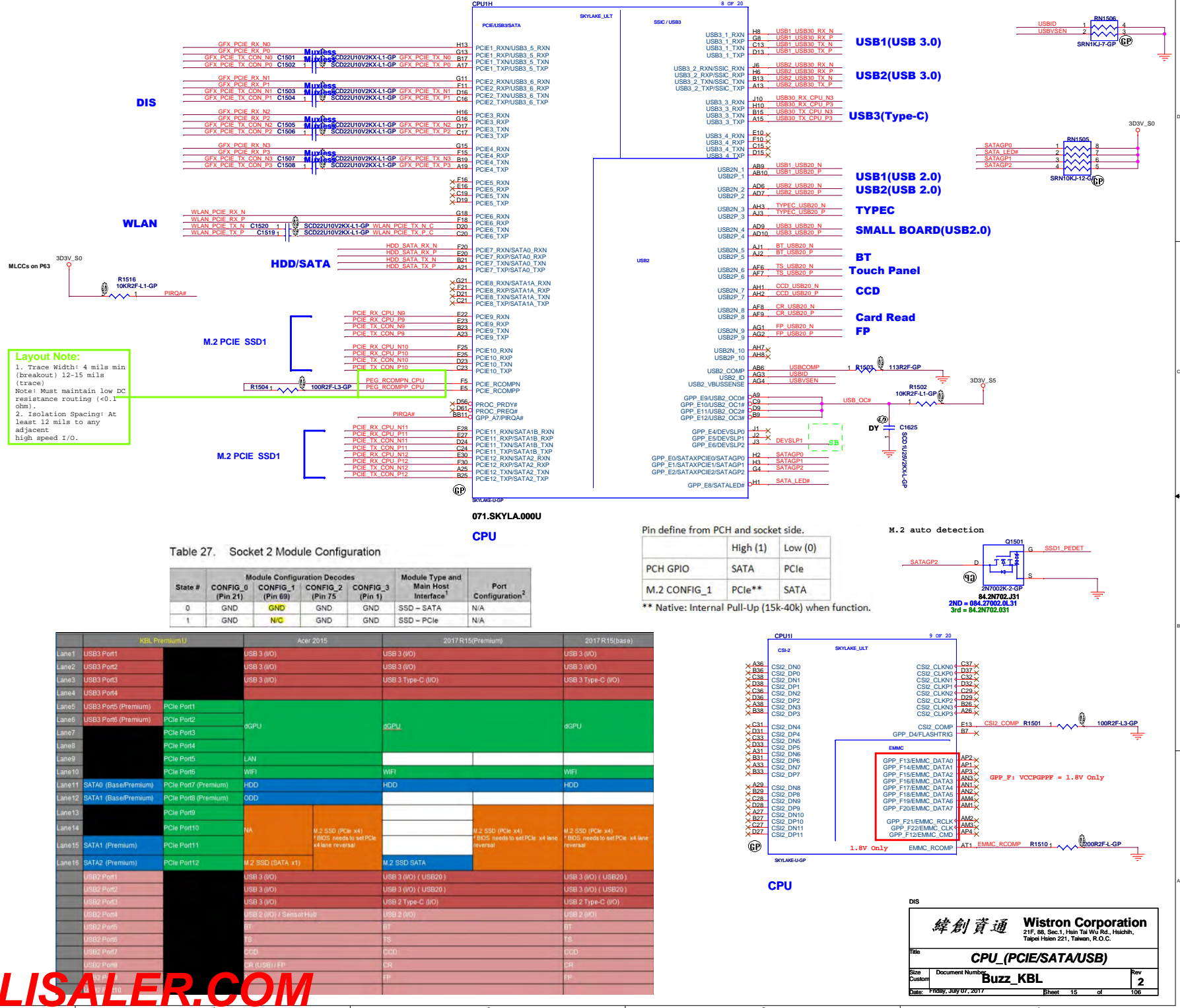
Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Drop Sx
HDA_AUDIO_INTERFACE					
HDA_BIST#	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	OFF
HDA_BIST#	Primary	Internal Pull- down	Driven Low	Internal Pull- down	OFF
HDA_BLK	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	OFF
HDA_SDO	Primary	Internal Pull- down	Driven Low	Driven Low	OFF
HDA_SDO[1:0]	Primary	Internal Pull- down	Internal Pull- down		OFF

## I/O Signal Planes and States

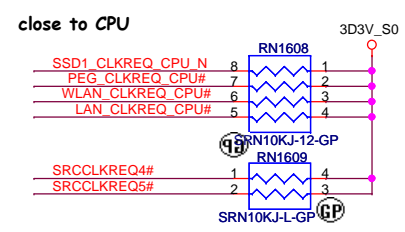
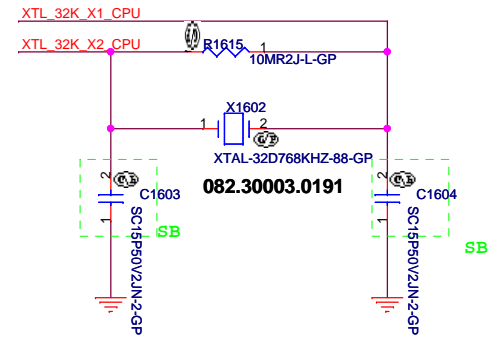
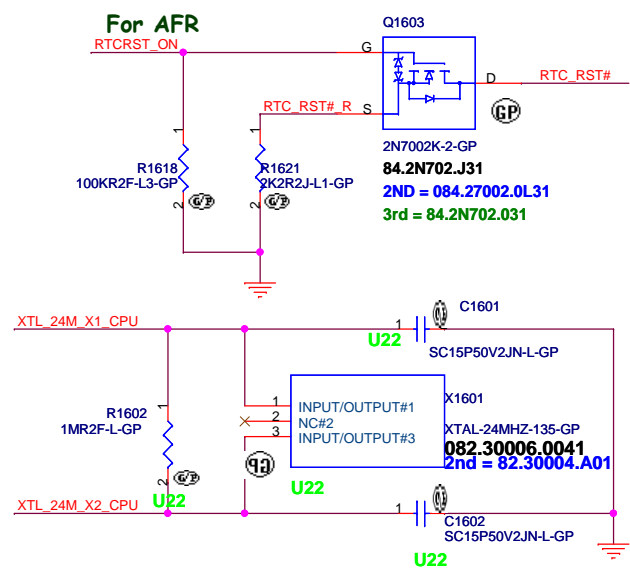
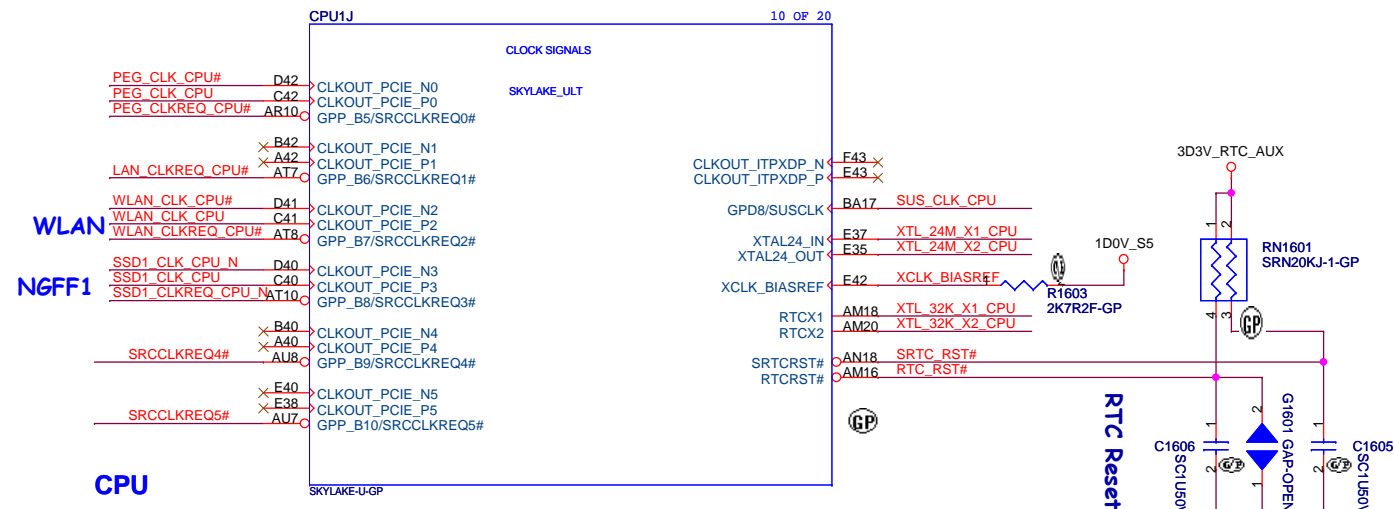
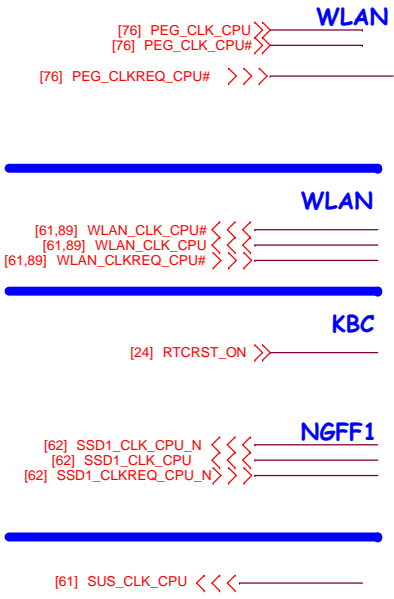
Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Drop Sx
SPI0_CLK	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	OFF
SPI0_MOSI	Primary	Internal Pull-up/ Pull-down (See Note 1 & 2)	Driven Low	Driven Low	OFF
SPI0_MISO	Primary	Internal Pull-up	Internal Pull-up	Internal Pull-up	OFF
SPI0_CS0#	Primary	Driven High (See Note 1)	Driven High	Driven High	OFF
SPI0_CS1#	Primary	Internal Pull-up (See Note 1)	Driven High	Driven High	OFF
SPI0_CS2#	Primary	Driven High (See Note 1)	Driven High	Driven High	OFF
SPI0_IO[2:1]	Primary	Internal Pull-up (See Note 1)	Internal Pull-up	Internal Pull-up	OFF
SPI1_CLK	Primary	Undriven	Undriven	Undriven	OFF
SPI1_MOSI	Primary	Undriven	Undriven	Undriven	OFF
SPI1_MISO	Primary	Undriven	Undriven	Undriven	OFF
SPI1_CS#	Primary	Undriven	Undriven	Undriven	OFF
SPI1_IO[2:1]	Primary	Undriven	Undriven	Undriven	OFF

Notes:  
1. Pins are tri-stated (with weak internal pull-up) prior to RSMRST# de-assertion.  
2. Weak internal pull-up resistor is enabled when RSMRST# is asserted and is switched to a weak internal pull-down when RSMRST# is de-asserted.

DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. Notes: 1. This internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. Notes: 1. This internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPT0_MOST / GPP_B18	No Reboot	Rising edge of PCH_PWRK	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h.Bit 5). 3. This signal is in the primary well.
GSPI1_MOST / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWRK	This signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory (readable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h.Bit 4)). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. 0 = SPI 1 = LPC Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h.Bit 5). 3. This signal is in the primary well.
signal	Usage	When Sampled	Comment
DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWRK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWRK	The signal has a weak internal pull-down. 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot block. PCH will invert A16 (default) for cycles going to the upper two cache blocks, in the VPH or the appropriate address lines (A16, A17, or A18) as selected in top swap block size soft strap (handled through FITC). Notes: 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Device33, Function0, Offset 0ch, Bit4). 4. This signal is in the primary well.
SMALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SMLOALERT# / GPP_C3	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.



Main Func = PCH



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Title MCP\_CLOCK

Size Custom Document Number Buzz\_KBL Rev 2

Date: Friday, July 07, 2017 Sheet 16 of 106

Main Func = PCH

### Audio Code

[17,27] HDA\_SYNC\_CODEEC <<<<—  
[17,27] HDA\_BITCLK\_CODEEC <<<<—  
[27] HDA\_SDOUT\_CODEEC <<<<—  
[27] HDA\_SDIN0\_CPU <<<<—  
[14,27] HDA\_SPKR <<<<—

[24] ME\_UNLOCK <<<<—

[17,27] HDA\_SYNC\_CODEEC <<<<—  
[17,27] HDA\_BITCLK\_CODEEC <<<<—

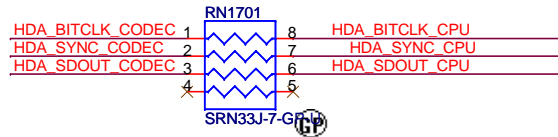
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[29] DMIC2\_CLK\_CPU <<<<—  
[29] DMIC1\_DATA\_CPU <<<<—  
[29] DMIC1\_CLK\_CPU <<<<—

3D3V\_S5  
R1702  
150KR2J-GP  
DY

HDA\_SDOUT\_CPU

1KR2F-L1-GP  
R1709  
ME\_UNLOCK

HDA\_SYNC\_CPU  
HDA\_BITCLK\_CPU  
HDA\_SDOUT\_CPU  
HDA\_SDIN0\_CPU



CPU1G

7 OF 20

AUDIO

SKYLAKE\_ULTRA

HDA\_SYNC/I2S0\_SFRM  
HDA\_BLK/I2S0\_SCLK  
HDA\_SDO/I2S0\_TXD  
HDA\_SDI0/I2S0\_RXD  
HDA\_SDI1/I2S1\_RXD  
HDA\_RST#/I2S1\_SCLK  
GPP\_D23/I2S\_MCLK  
I2S1\_SFRM  
I2S1\_TXD

GPP\_F1/I2S2\_SFRM  
GPP\_F0/I2S2\_SCLK  
GPP\_F2/I2S2\_TXD  
GPP\_F3/I2S2\_RXD

1.8V Only

DMIC1\_CLK\_CPU  
DMIC1\_DATA\_CPU

H5  
D7  
GPP\_D19/DMIC\_CLK0  
GPP\_D20/DMIC\_DATA0

DMIC2\_CLK\_CPU  
DMIC2\_DATA\_CPU

D8  
C8  
GPP\_D17/DMIC\_CLK1  
GPP\_D18/DMIC\_DATA1

HDA\_SPKR

AW5  
GPP\_B14/SPKR

SDIO/SDXC

GPP\_G0/SD\_CMD  
GPP\_G1/SD\_DATA0  
GPP\_G2/SD\_DATA1  
GPP\_G3/SD\_DATA2  
GPP\_G4/SD\_DATA3  
GPP\_G5/SD\_CD#  
GPP\_G6/SD\_CLK  
GPP\_G7/SD\_WP

AB11  
AB13  
AB12  
W12  
W11  
W10  
W8  
W7

GPP\_A17/SD\_PWR\_EN#/ISH\_GP7  
GPP\_A16/SD\_1P8\_SEL

BA9  
BB9

SD\_RCOMP

1.8V Only

GPP\_F23

AF13

R1701  
200R2F-L-GP  
DY

SKYLAKE-U-GP

CPU

## 18.3 Terminating Unused SDXC Signals

SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD\_RCOMP pin does not need to be connected to a RCOMP resistor.

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Size Custom Document Number  
**Buzz\_KBL**

Rev  
**2**

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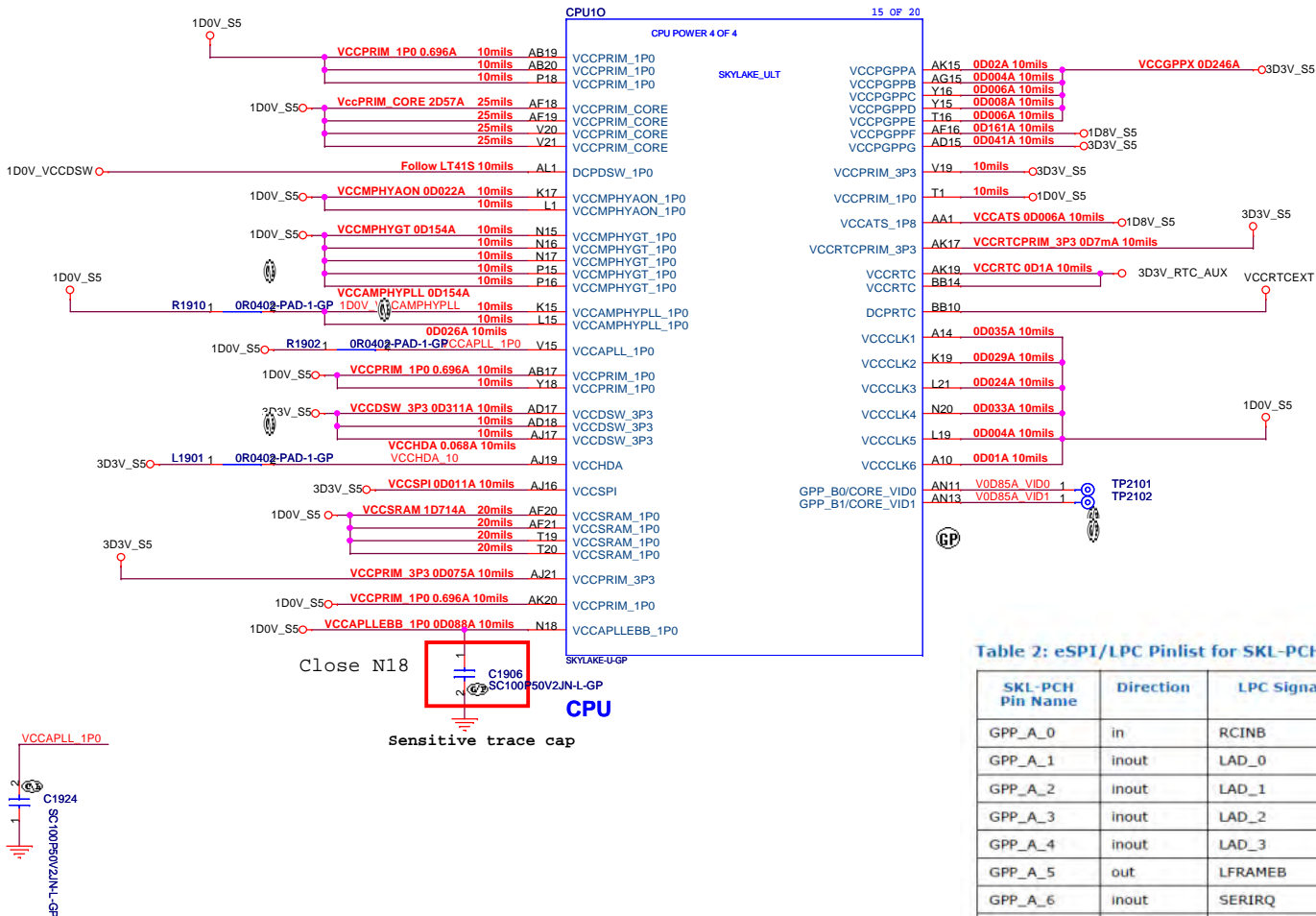


Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SM LOALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

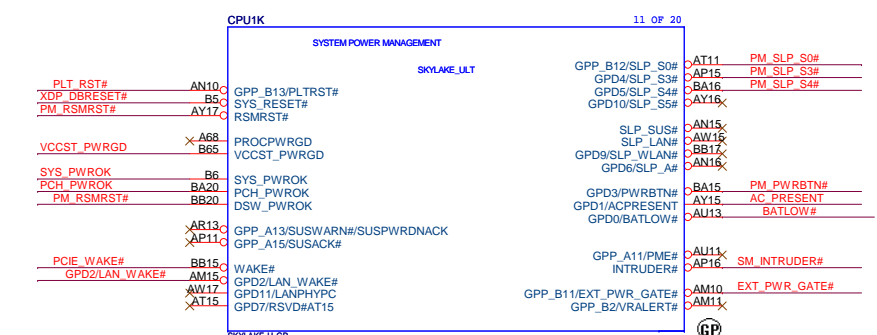
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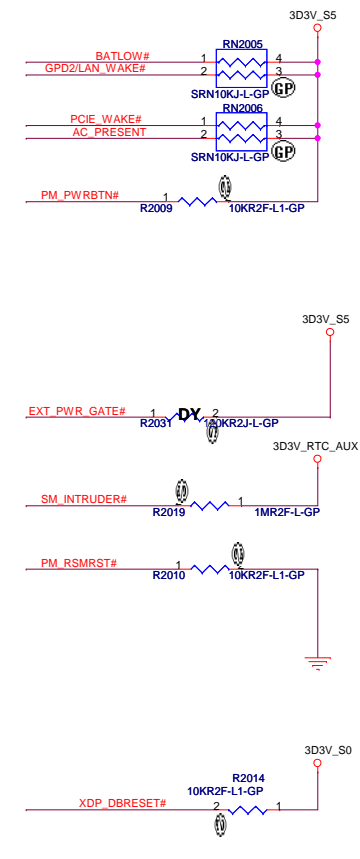
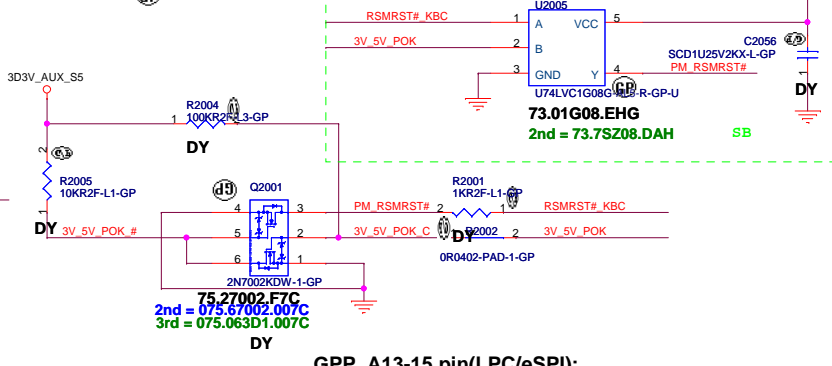
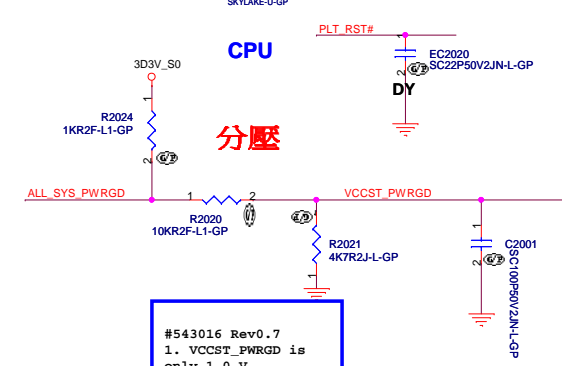
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SizeCustomDocument NumberBuzz\_KBLRev2  
DateFriday, July 07, 2017Sheet19 of106

Main Func = PCH

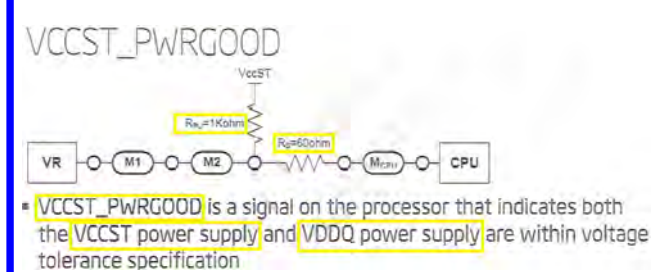
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[40] PCH\_PWROK >>>  
[24,61,62] PCIE\_WAKE# >>>  
[24,40] ALL\_SYS\_PWRGD >>>  
[24,61,62,68,79,89,91] PLT\_RST# <<<  
[24] RSMRST#\_KBC >>>  
[45,53,73] 3V\_5V\_POK >>>  
[24,40,45] PM\_SLP\_S3# <<<  
[24,40,51] PM\_SLP\_S4# <<<  
[24] PM\_PWRBTN# >>>  
[24] AC\_PRESENT >>>  
[40,60,91] PM\_SLP\_S0# >>>



BATLOW#:  
Pull-up required even if not implemented.



Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWARN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)



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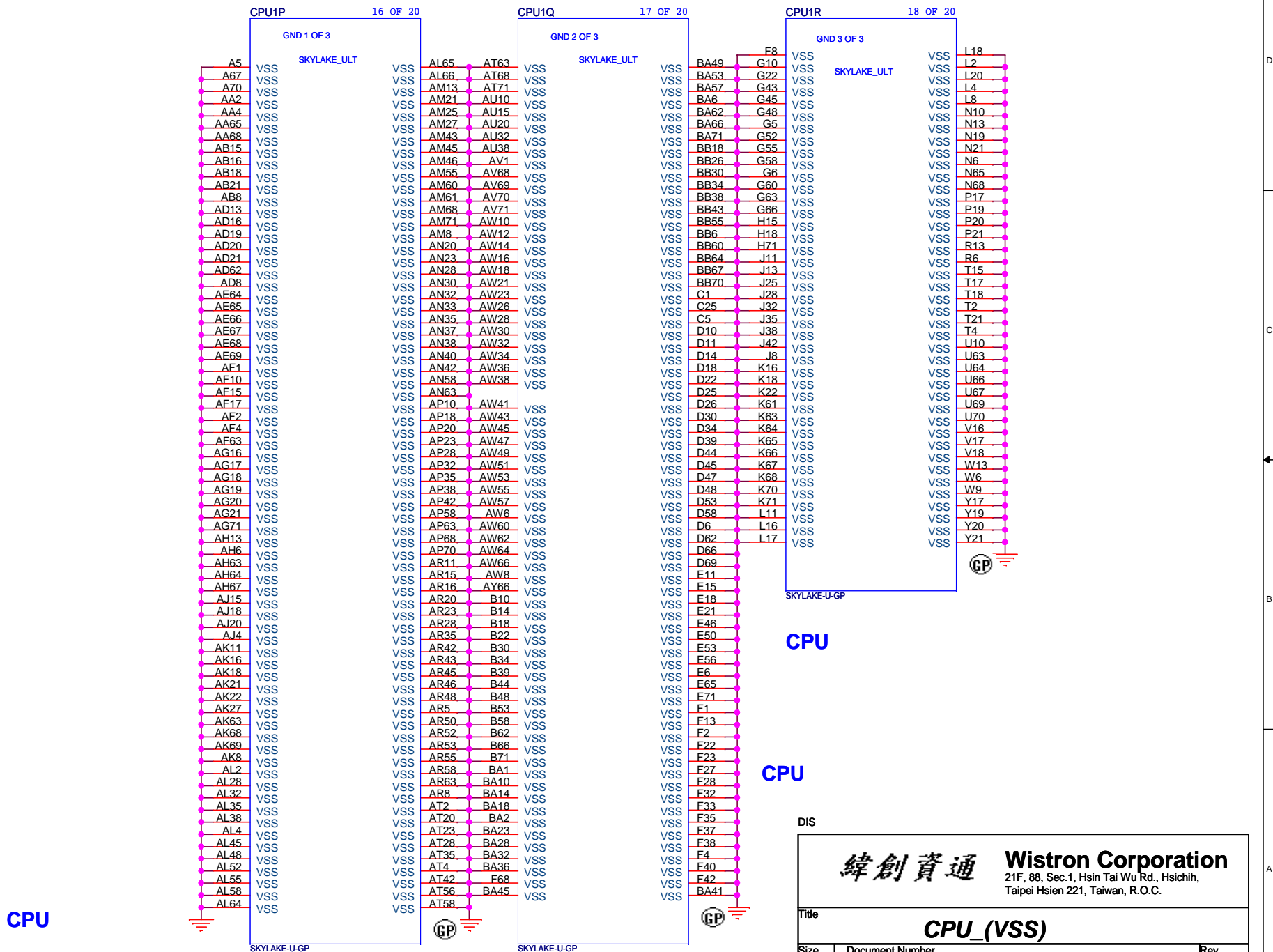
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File CPU\_(POWER MANAGEMENT)

Size Custom Document Number Buzz\_KBL Rev 2

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Main Func = PCH



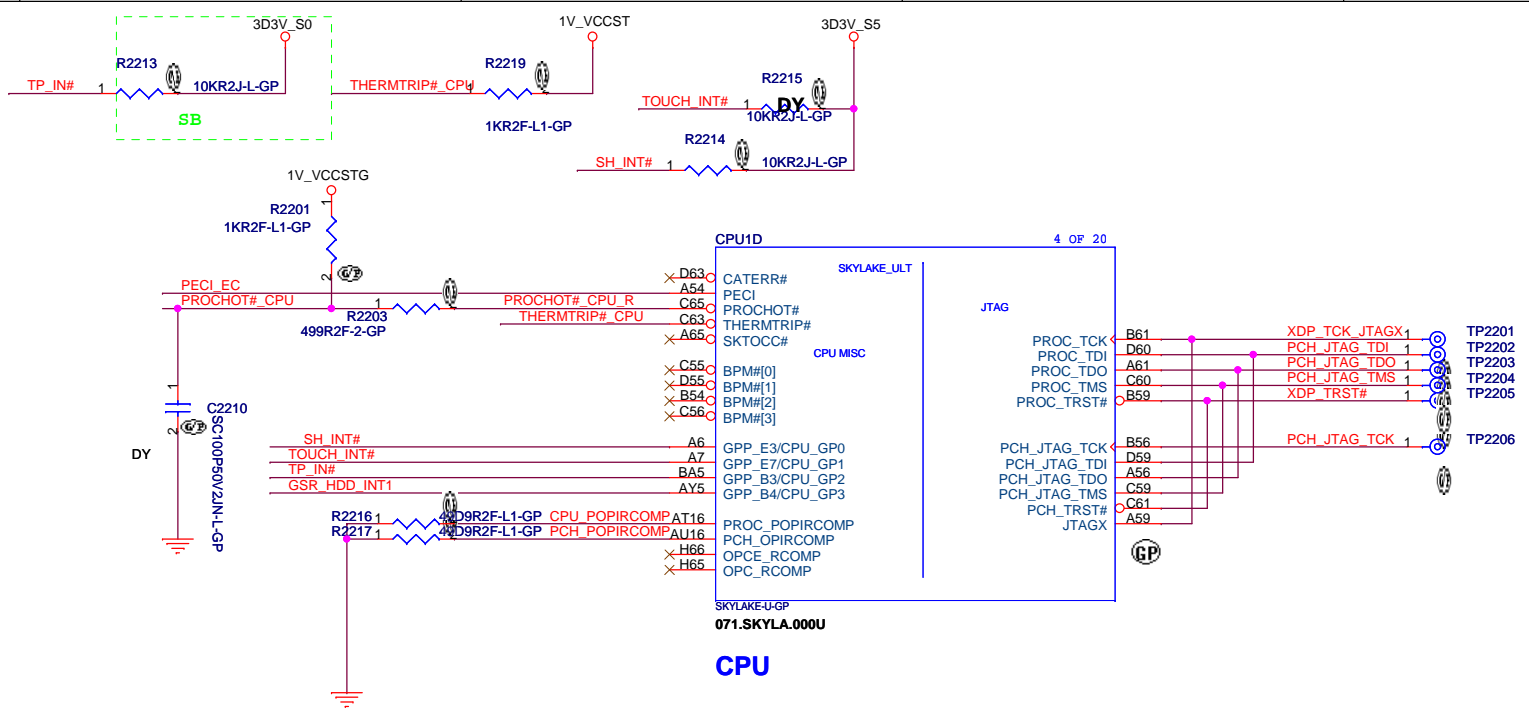
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Size Custom	Document Number Buzz_KBL	Rev 2
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Main Func = CPU

- [24] PECL\_EC << >>—
- [24,44,46] PROCHOT#\_CPU << >>—
- [24] SH\_INT# >>>—
- [55] TOUCH\_INT# >>>—
- [65] TP\_IN# >>>—
- [69] GSR\_HDD\_INT1 >>>—



PROCHOT#	<b>Processor Hot:</b> PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD 0	SE	All processor lines
THERMTRIP#	<b>Thermal Trip:</b> The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	0	OD	SE	All processor lines

DIS

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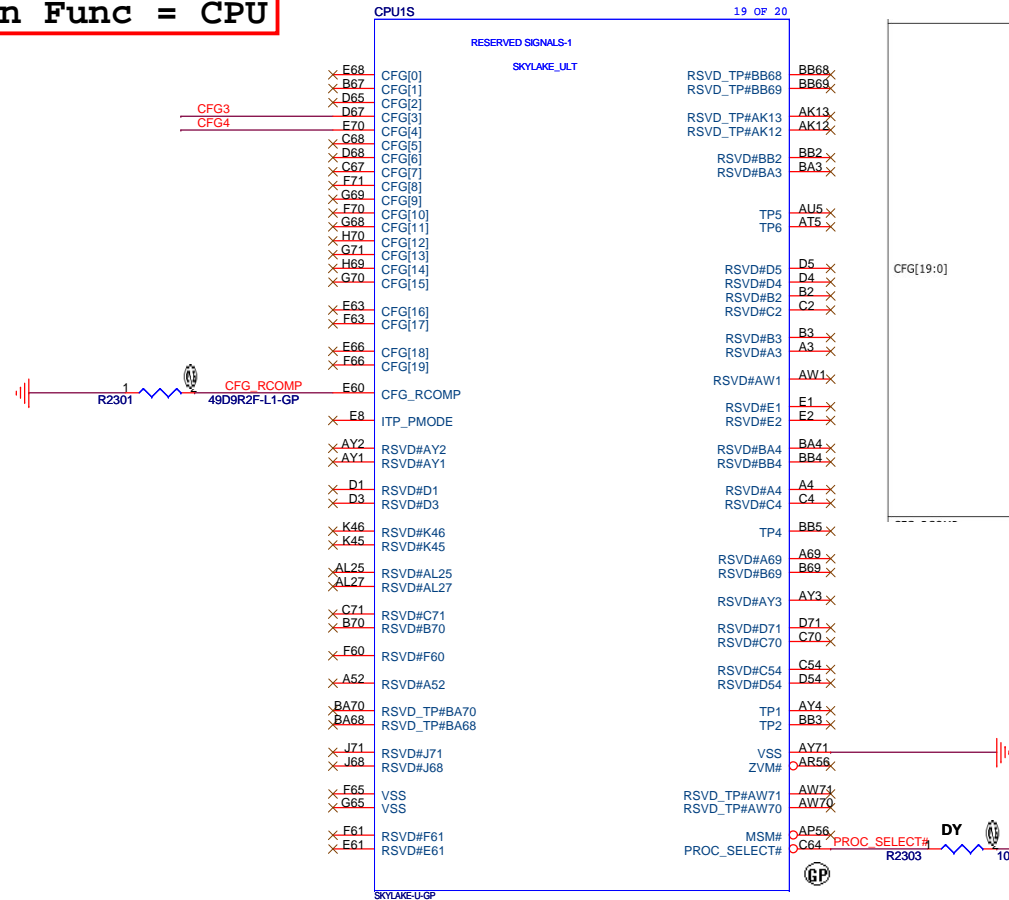
Wistron Corporation

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Title **CPU (JTAG/CPU SIDE BAND)**

Size Custom	Document Number <b>Woody KBL</b>	Rev <b>2</b>
Date: Friday, July 07, 2017	Sheet 22 of 106	

# Main Func = CPU

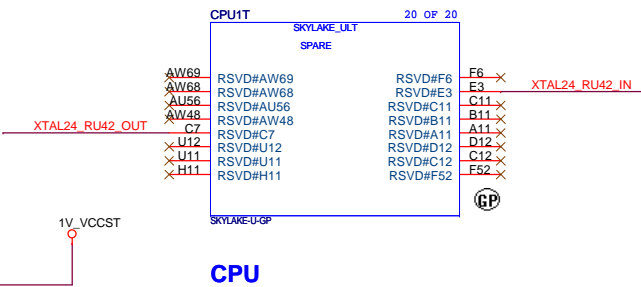


**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

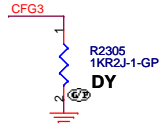
Intel recommends placing test points on the board for CFG pins.

- |   |                                 |   |
|---|---------------------------------|---|
| <ul style="list-style-type: none"> <li>• <b>CFG[0]:</b> Stall reset sequence after PCU PLL lock until de-asserted:             <ul style="list-style-type: none"> <li>– 1 = (Default) Normal Operation; No stall.</li> <li>– 0 = Stall.</li> </ul> </li> <li>• <b>CFG[1]:</b> Reserved configuration lane.</li> <li>• <b>CFG[2]:</b> PCI Express* Static x16 Lane Numbering Reversal.             <ul style="list-style-type: none"> <li>– 1 = Normal operation</li> <li>– 0 = Lane numbers reversed.</li> </ul> </li> <li>• <b>CFG[3]:</b> Reserved configuration lane.</li> <li>• <b>CFG[4]:</b> eDP enable:             <ul style="list-style-type: none"> <li>– 1 = Disabled.</li> <li>– 0 = Enabled.</li> </ul> </li> <li>• <b>CFG[6:5]:</b> PCI Express* Bifurcation             <ul style="list-style-type: none"> <li>– 00 = 1 x8, 2 x4 PCI Express*</li> <li>– 01 = reserved</li> <li>– 10 = 2 x8 PCI Express*</li> <li>– 11 = 1 x16 PCI Express*</li> </ul> </li> <li>• <b>CFG[7]:</b> PEG Training:             <ul style="list-style-type: none"> <li>– 1 = (default) PEG Train immediately following RESET# de assertion.</li> <li>– 0 = PEG Wait for BIOS for training.</li> </ul> </li> <li>• <b>CFG[19:8]:</b> Reserved configuration lanes.</li> </ul> | <p>I/O</p> <p>GTL</p> <p>SE</p> | <p>All processor lines.</p> <p>CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.</p> |
|---|---------------------------------|---|

E All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

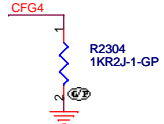


**PCH strap pin:**

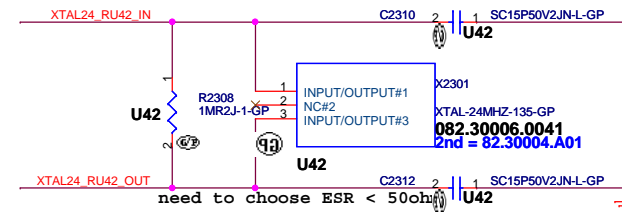


[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

**PCH strap pin:**



DISPLAY PORT PRESENCE STRAP	
CFG[4]	<p>0 : ENABLED            An external Display Port device is connected to the Embedded Display Port.</p> <p>1 : DISABLED (Default)            No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.</p>



PROC_SELECT#	<b>Processor Select:</b> This pin is for compatibility with future platforms. It should be unconnected for SK1.			N/A	All processor lines
--------------	---	--	--	-----	---------------------

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Title	<b><i>CPU_RESERVED,CFG</i></b>
-------	--------------------------------

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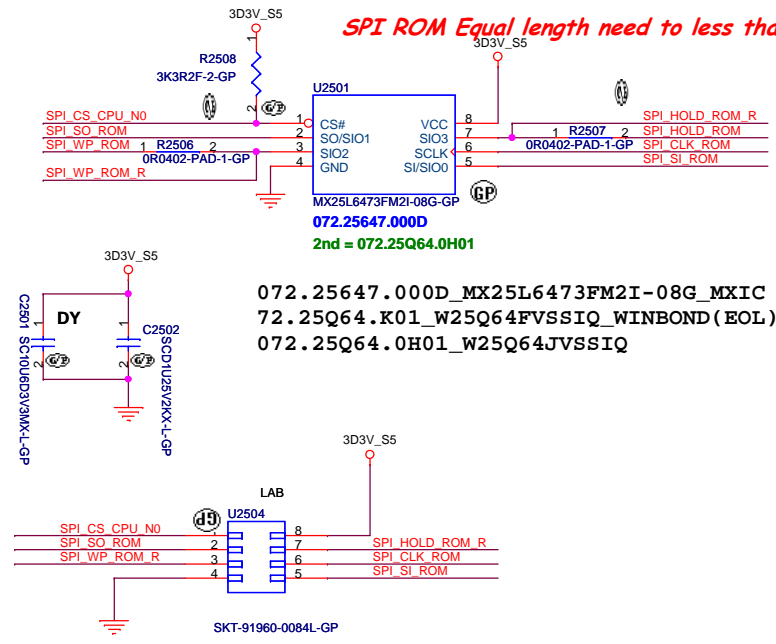


[18,24] SPI\_CS\_CPU\_N0  
[18,24] SPI\_SO\_ROM  
[18] SPI\_WP\_ROM  
[14] SPI\_WP\_ROM\_R  
[14] SPI\_HOLD\_ROM\_R  
[18] SPI\_HOLD\_ROM  
[18,24] SPI\_CLK\_ROM  
[18,24] SPI\_SI\_ROM  
[6] RTC\_DET#

# Main Func = SPI Flash

## SPI FLASH ROM (8M byte) for PCH

*SPI ROM Equal length need to less than 500mil*



[illegible]

```
VD_IN1  trace 10 mli
```

[89] FAN\_TACH2\_C <<<\_\_\_\_\_

**\*Layout\* 15 mil**

**5V\_S0**

**DY**

**D2601**  
RB551V30-GP  
**83.R5003.H8H**  
**2ND = 83.R5003.T8F**

**C2603**  
ICADU25/50X-L2-GP

**C2602**  
ICADU25/50X-L2-GP

**FAN1**

**FAN1\_PWM**  
**FAN1\_TACH1**  
**83.R5003.H8H**  
**2ND = 83.R5003.T8F**

**D2602**  
RB551V30-GP

**FAN1\_TACH1\_C**

**D2603**  
RB551V30-GP

**FAN1\_TACH2\_C**

**FAN2\_PWM**  
**83.R5003.H8H**  
**2ND = 83.R5003.T8F**

**5V\_S0**

**FAN1**

**SB**  
**20.F2191.008**  
**2ND = 20.F1261.008**

**ACES-CON8-44-GP**

Size	Document Number	Rev
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A4

Document Number

**Buzz KBL**

Rev  
**2**

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SSID = AUDIO

Speaker

[18,27] SML0\_CLK\_CPU >>>  
[18,27] SML0\_DATA\_CPU <<<  
[27] Smart\_AMP\_MCLK >>>  
[27] Smart\_AMP\_BCLK >>>  
[27] Smart\_AMP\_LRCK >>>  
[27] Smart\_AMP\_DIN >>>  
[27] Smart\_AMP\_DOUT <<<  
[27] AMP\_PD >>>  
[27] AUD\_SPK1\_R\_L- >>>  
[27] AUD\_SPK1\_R\_L+ >>>  
[27] AUD\_SPK1\_R\_R- >>>  
[27] AUD\_SPK1\_R\_R+ >>>

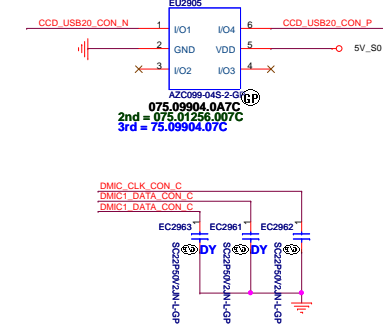
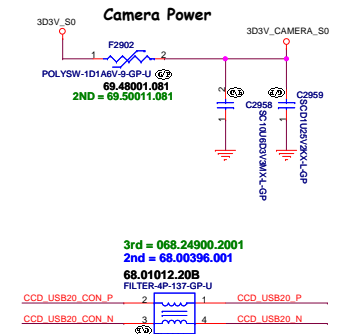
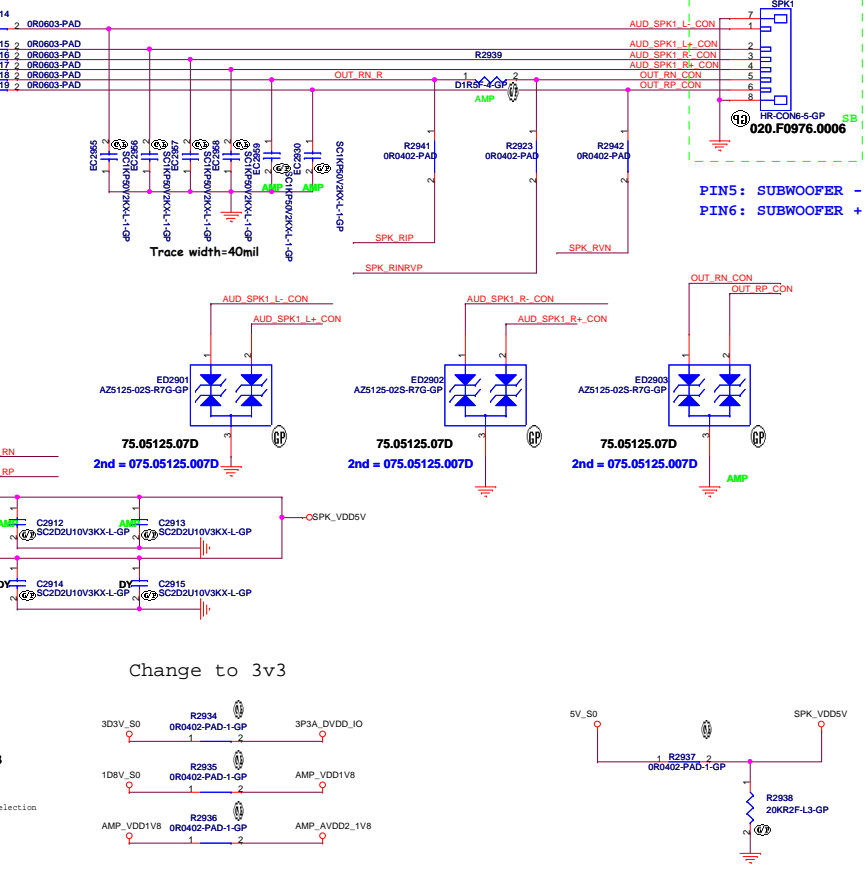
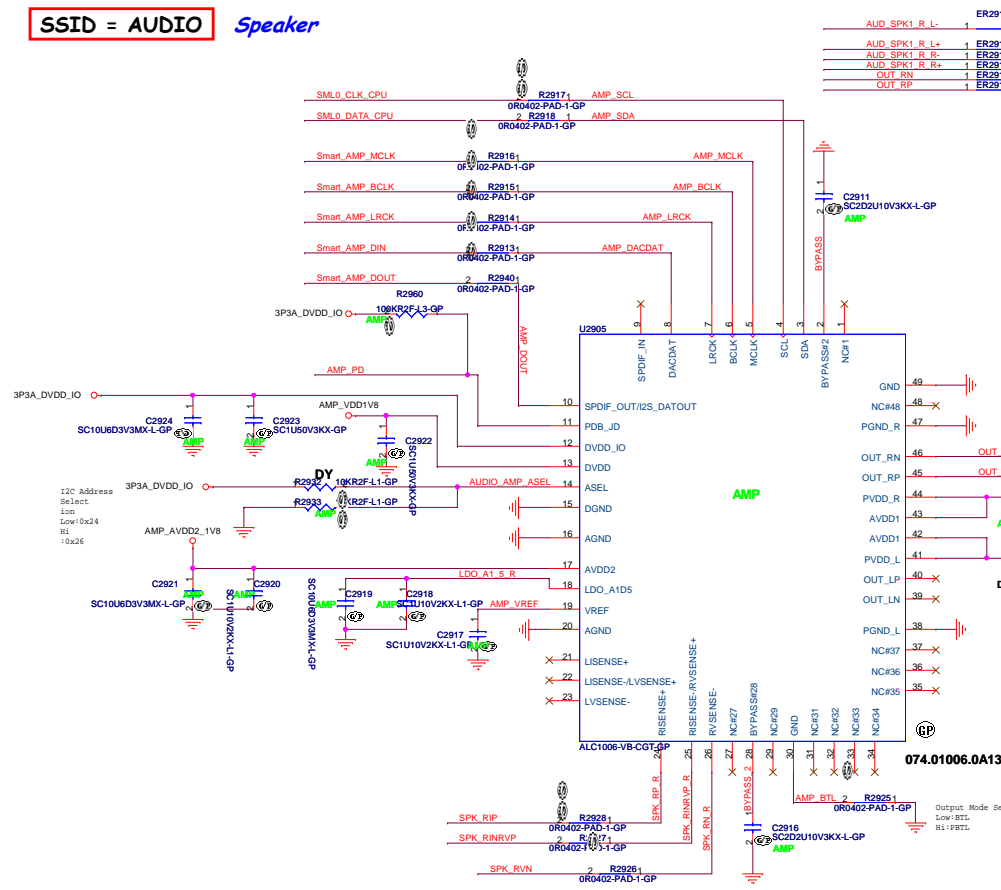
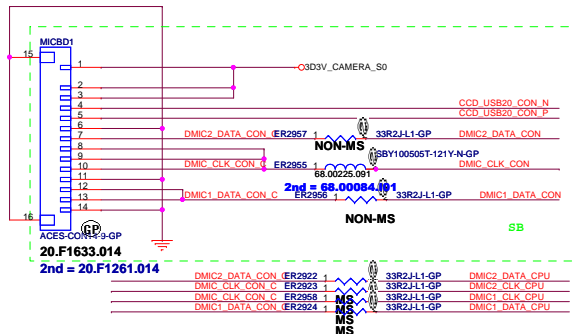
[89] AUD\_SPK1\_L-CON >>>  
[89] AUD\_SPK1\_L+CON >>>  
[89] AUD\_SPK1\_R-CON >>>  
[89] AUD\_SPK1\_R+CON >>>  
[89] OUT\_RN\_CON >>>  
[89] OUT\_RP\_CON >>>

[17] DMIC2\_CLK\_CPU <<<  
[17] DMIC2\_DATA\_CPU <<<  
[17] DMIC1\_CLK\_CPU <<<  
[17] DMIC1\_DATA\_CPU <<<

[89] CCD\_USB20\_CON\_P <<<  
[89] CCD\_USB20\_CON\_N <<<  
[89] DMIC\_CLK\_CON\_C <<<  
[89] DMIC1\_DATA\_CON\_C <<<  
[89] DMIC2\_DATA\_CON\_C <<<

[27] DMIC\_CLK\_CON <<<  
[27] DMIC1\_DATA\_CON <<<  
[27] DMIC2\_DATA\_CON <<<

[15] CCD\_USB20\_P <<<  
[15] CCD\_USB20\_N <<<



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<b>(LAN+VGA) CONNECTOR</b>					
Size	Document Number				Rev
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RTS5170(CARD READER)	
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SSID = SDIO

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Size A4	Document Number <b>Buzz KBL</b>				Rev <b>2</b>
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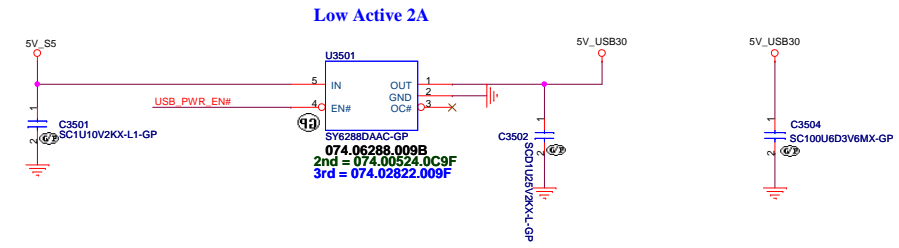
[15] USB1\_USB20\_N << >>  
 [15] USB1\_USB20\_P << >>  
 [24,35,64] USB\_PWR\_EN# << >>  
 [15] USB1\_USB30\_RX\_N << >>  
 [15] USB1\_USB30\_RX\_P << >>  
 [15] USB1\_USB30\_TX\_N << >>  
 [15] USB1\_USB30\_TX\_P << >>  
 [24,35,64] USB\_PWR\_EN# << >>

[89] USB1\_CON\_USB20\_N << >>  
 [89] USB1\_CON\_USB20\_P << >>

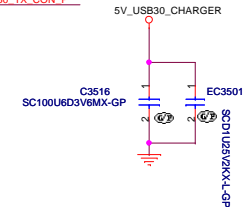
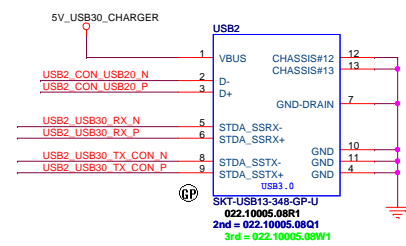
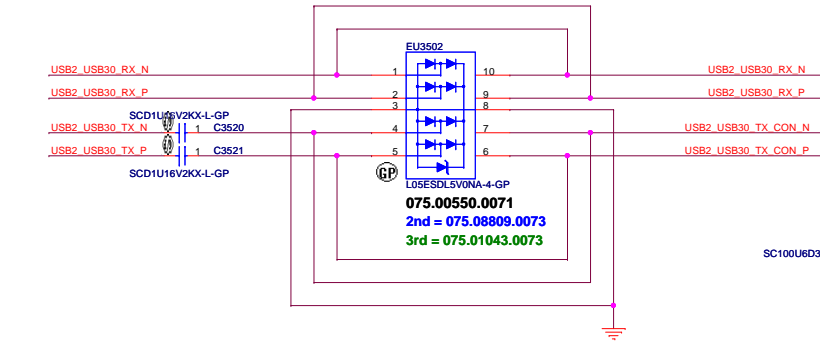
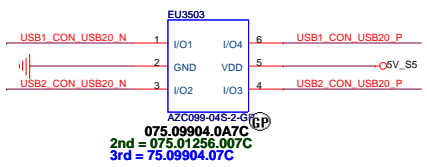
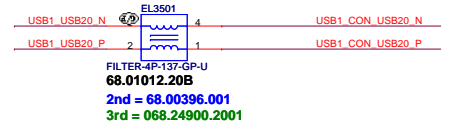
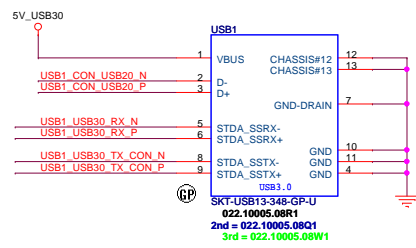
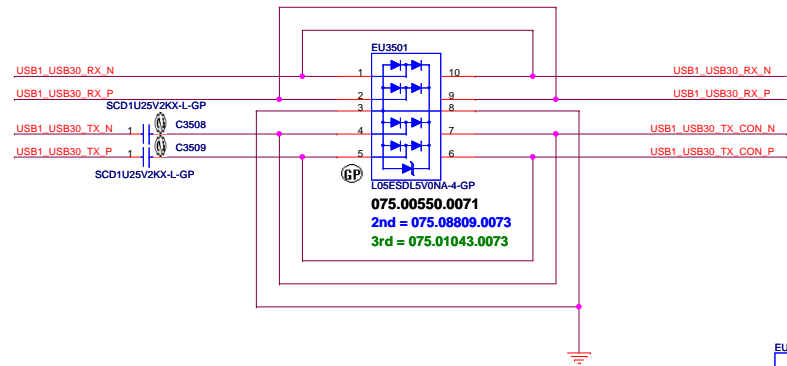
[36] USB2\_CHAR\_N << >>  
 [36] USB2\_CHAR\_P << >>

[15] USB2\_USB30\_RX\_N << >>  
 [15] USB2\_USB30\_RX\_P << >>  
 [15] USB2\_USB30\_TX\_N << >>  
 [15] USB2\_USB30\_TX\_P << >>

[89] USB2\_CON\_USB20\_N << >>  
 [89] USB2\_CON\_USB20\_P << >>



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX



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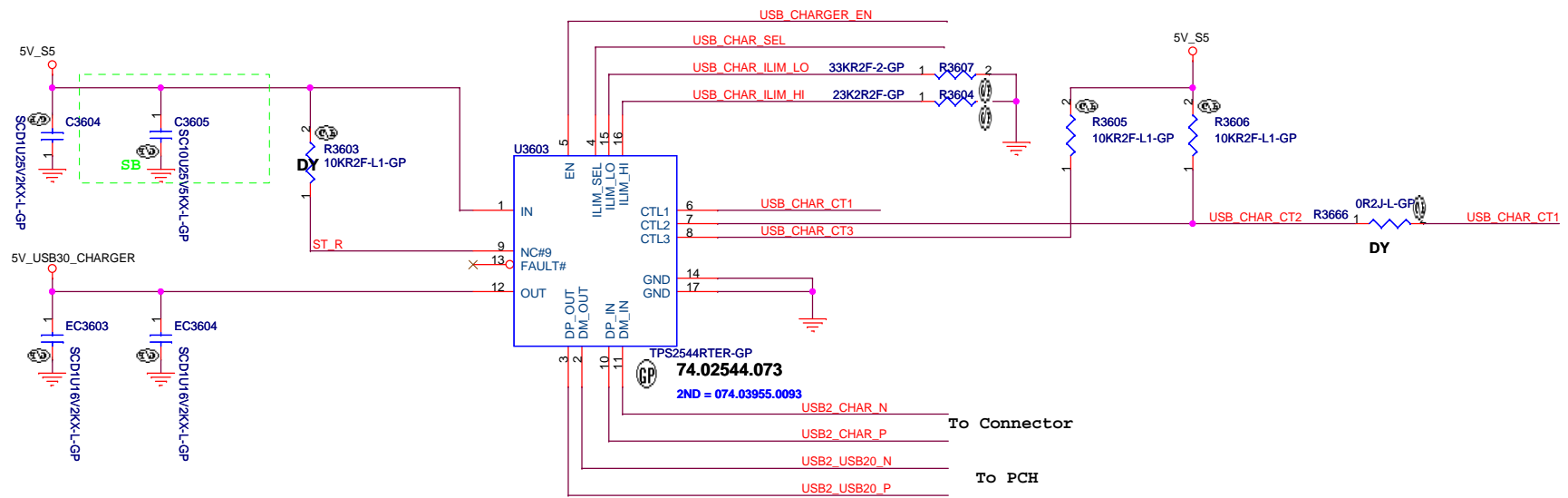
[24] USB\_CHARGER\_EN >>>  
[24] USB\_CHAR\_SEL >>>  
[24] USB\_CHAR\_CT1 >>>

To Connector

[35] USB2\_CHAR\_N <<<  
[35] USB2\_CHAR\_P <<<

To PCH

[15] USB2\_USB20\_N <<<  
[15] USB2\_USB20\_P <<<



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 <sup>(1)</sup>	ILIM_LO	
1	1	1	1	CDP <sup>(1)</sup>	ILIM_HI	Data Lines Connected

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TitleReserved		
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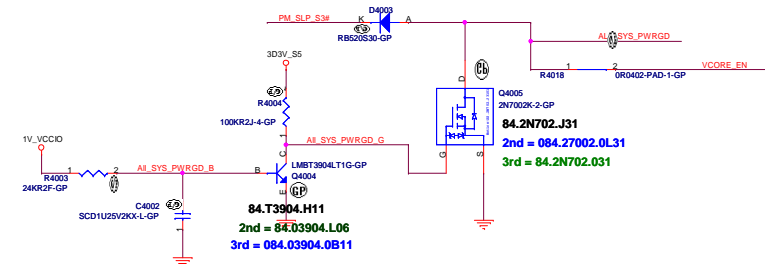
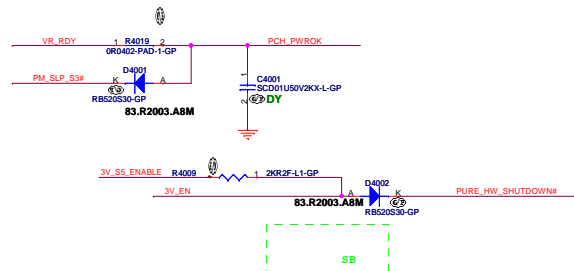
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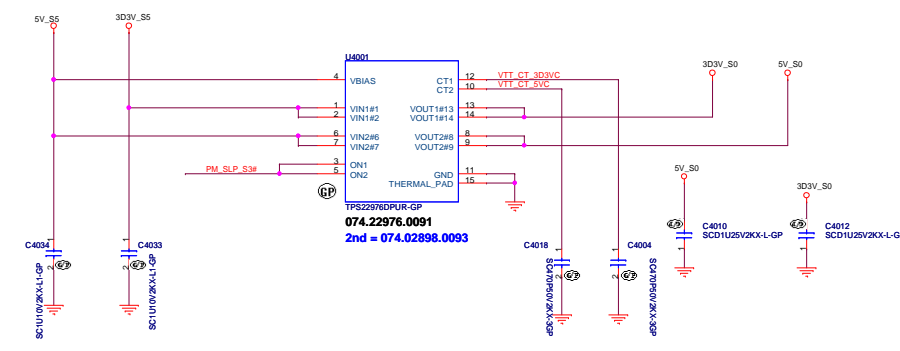
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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# Power Sequence

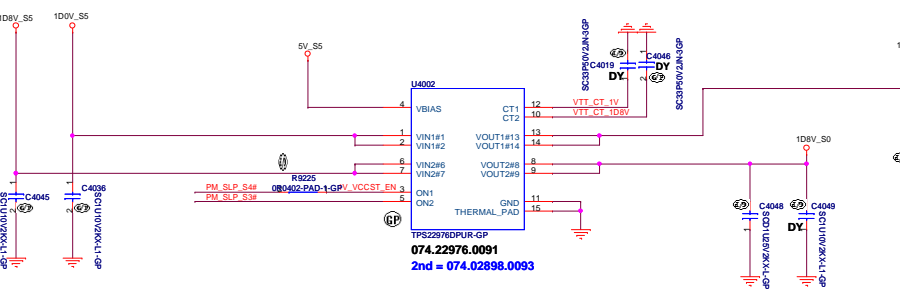
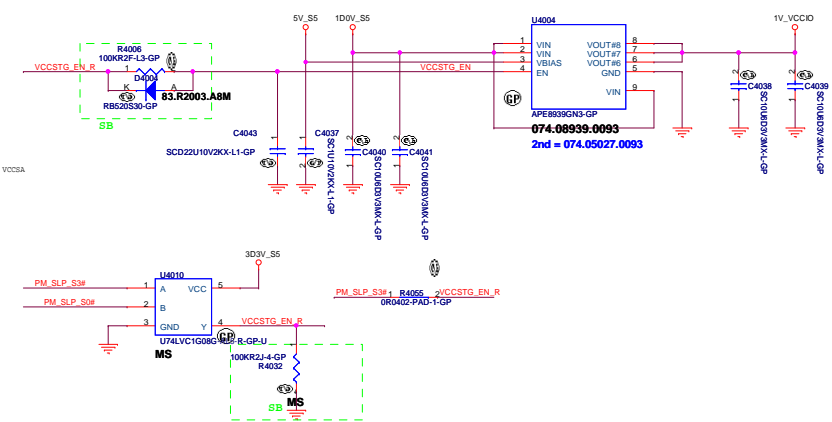
[26,46] VR\_RDY >>>  
 [20,24,45] PM\_SLP\_S3W >>>  
 [20] PCH\_PWROK <<<  
 [24] 3V\_S5\_ENABLE <<<  
 [45] 3V\_EN <<<  
 [24,26] PURE\_HW\_SHUTDOWN# >>>  
 [20,24] ALL\_SYS\_PWRGD <<<  
 [46] VCORE\_EN <<<  
 [20,24,51] PM\_SLP\_S4W >>>  
 [20,60,91] PM\_SLP\_S0W >>>



## ANNIE Run Power



1136 Simon  
 Tuning RC for DRAM  
 VCCIO = SLP\_S3  
 2.5V = SLP\_S4  
 VCCIO effect VCCSA  
 Sequence should  
 D0R4 =  
 SLP\_S4 > 2.5V > VDDQ > VCCIO > VCCSA  
 D0R3 =  
 SLP\_S4 > VDDQ > VDDIO > VDDSA  
 D0R4  
 R4006 = 100K  
 C4043 = 0.22u  
 D5702 = stuff  
 D0R3  
 R4006 = 33K  
 C4043 = 0.1u  
 D5702 = stuff



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Title		Power Plane Enable & SEQUENCE	
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TitleDCIN JACK		
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[24] AD\_OFF >>>\_\_\_\_\_

[24,44] BAT\_IN# <<< \_\_\_\_\_  
[24,44] BAT\_SCL <<< \_\_\_\_\_  
[24,44] BAT\_SDA <<< \_\_\_\_\_

[43,89] BAT\_G <<< \_\_\_\_\_

[89] BAT\_IN#\_1 <<< \_\_\_\_\_  
[89] BATA\_SCL\_1 <<< \_\_\_\_\_  
[89] BATA\_SDA\_1 <<< \_\_\_\_\_

[64] BAT\_RST <<< \_\_\_\_\_

[74] AC\_DET <<<\_\_\_\_\_

DCIN1

7

1

2

3

4

5

6

8

ETY-CON6-36-GP

19V\_AD\_JK

PC4304

PC4305

PD4304

P6SMBJ20A-GP-1

83.P6SMB.AAG

2nd = 083.00020.00AG

3rd = 83.P6SMB.EAG

SCD1U50V3KX-L-GP

R4301

470KR3J-L2-GP

AC\_DET

R4302

75KR3F-GP

EC4301

SC10U25V5KX-L-GP

DY

AD OFF 1

LTC024EUB GP GP

84.00024.A1K

2ND = 84.05212.B11

3rd = 84.01303.H1K

2ND = 84.02303.01K  
3rd = 084.05112.001K

1st = 84.08131.037  
2nd = 084.03307.0037

**BATTERY CONNECTOR**

BT+ O

PC4301 PC4302

SC01U25V/2KX-L-GP

SC01U25V/2KX-L-GP

BAT IN# 4

BAT SCL 3

BAT SDA 2

PN4301

SRN33J-7-GP-U

BAT IN# 1 5

BATA SCL 1 6

BATA SDA 1 7

BTY1

ACES-CON8-53-GP

20.F2132.008

2nd = 020.F0043.0008

3D3V\_RTC\_AUX

PR4301

1MR2J-L3-GP

BAT\_RST

84.2N702.J31

2nd = 084.27002.0L31

3rd = 84.2N702.031

BAT\_G [43.89]

PR4305

0R2J-L-GP

LAB

BI SW

————>>> BAT\_G [43,89]

84.2N702.J31  
2nd = 084.27002.0L31  
3rd = 84.2N702.031

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Title

**BATT CONN**

Size	Custom
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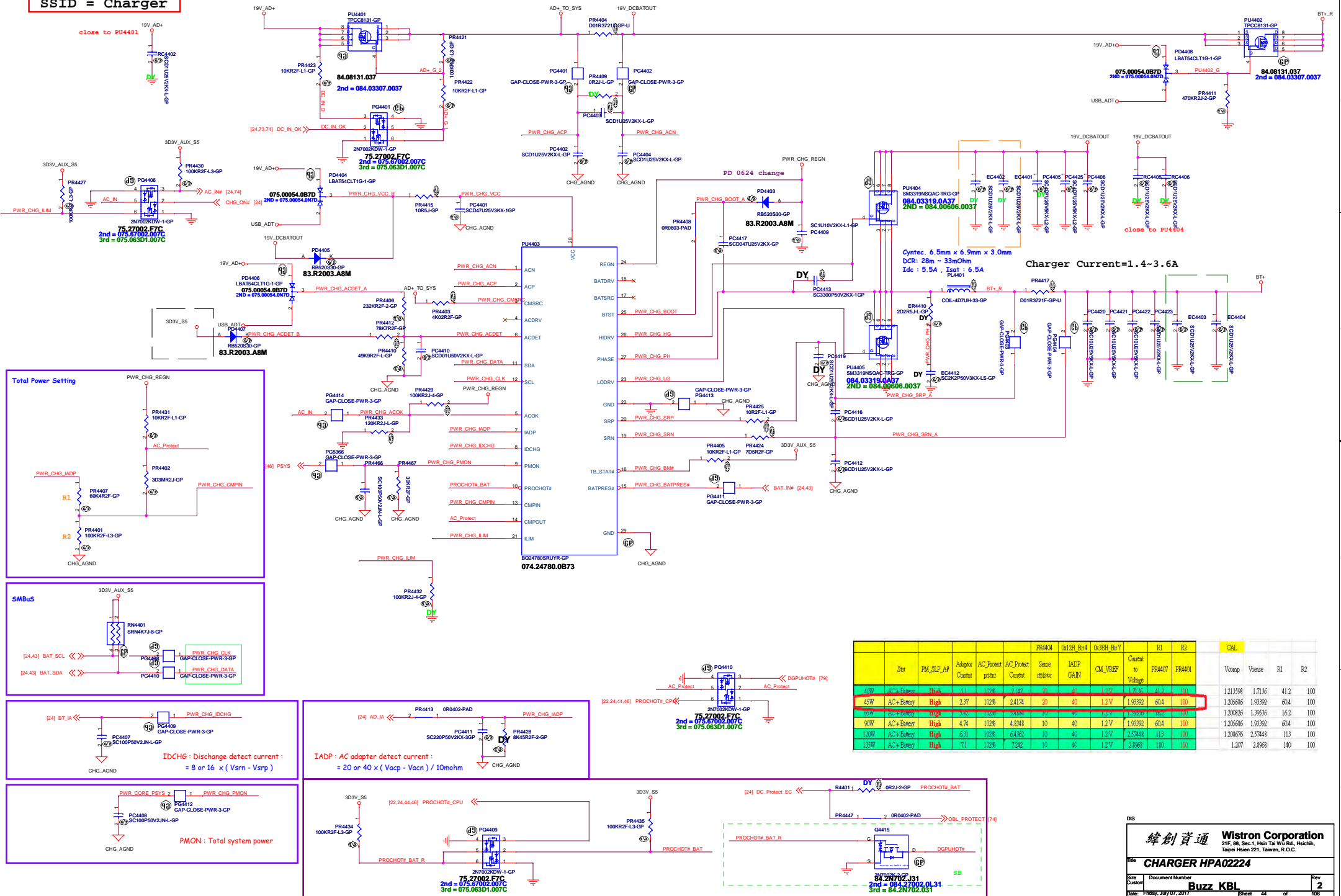
Document Number

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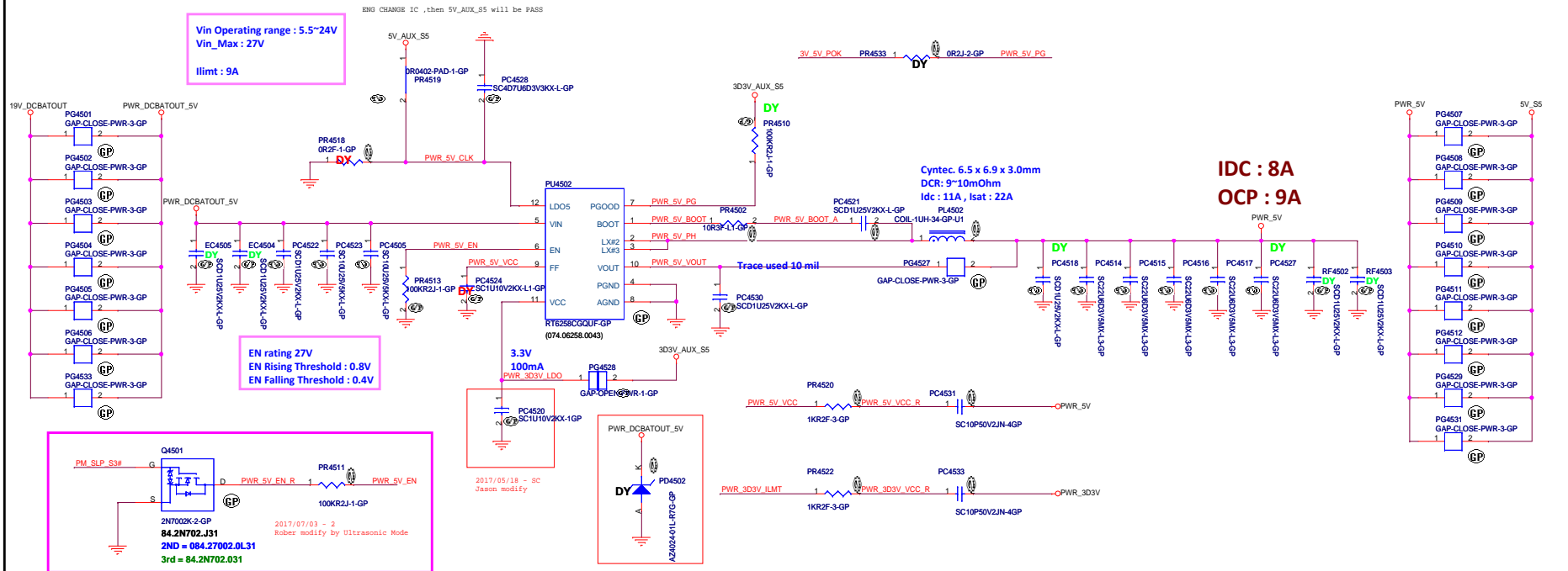
Date: Friday, July 07, 2017

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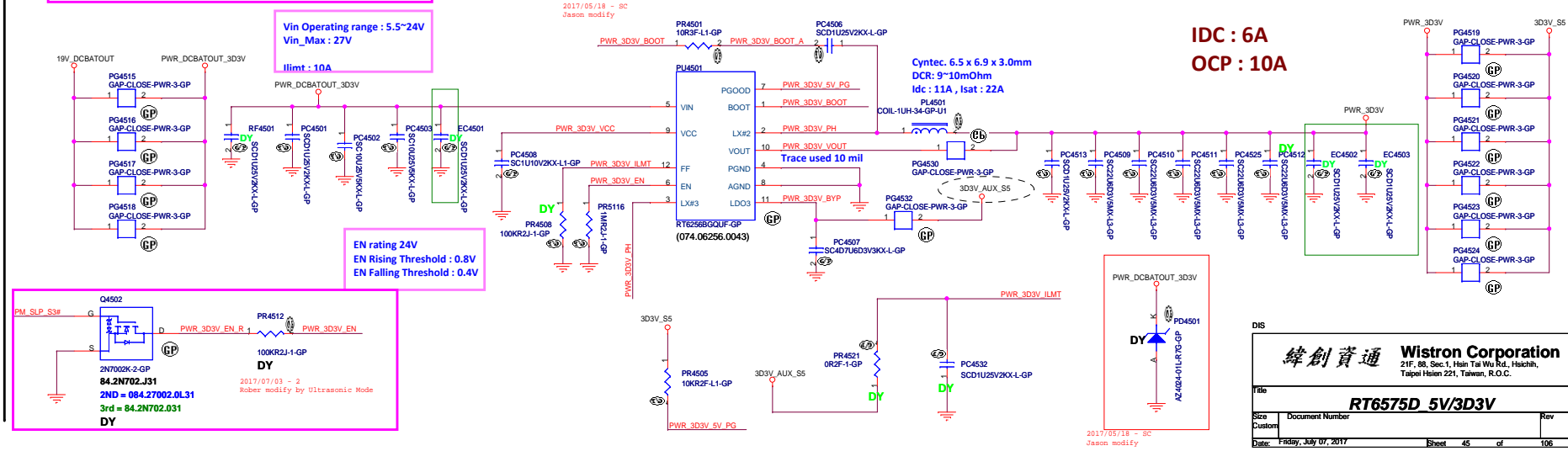
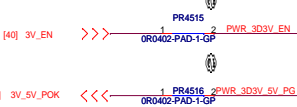
SSID = Charger



OFFPAGE



OFFPAGE

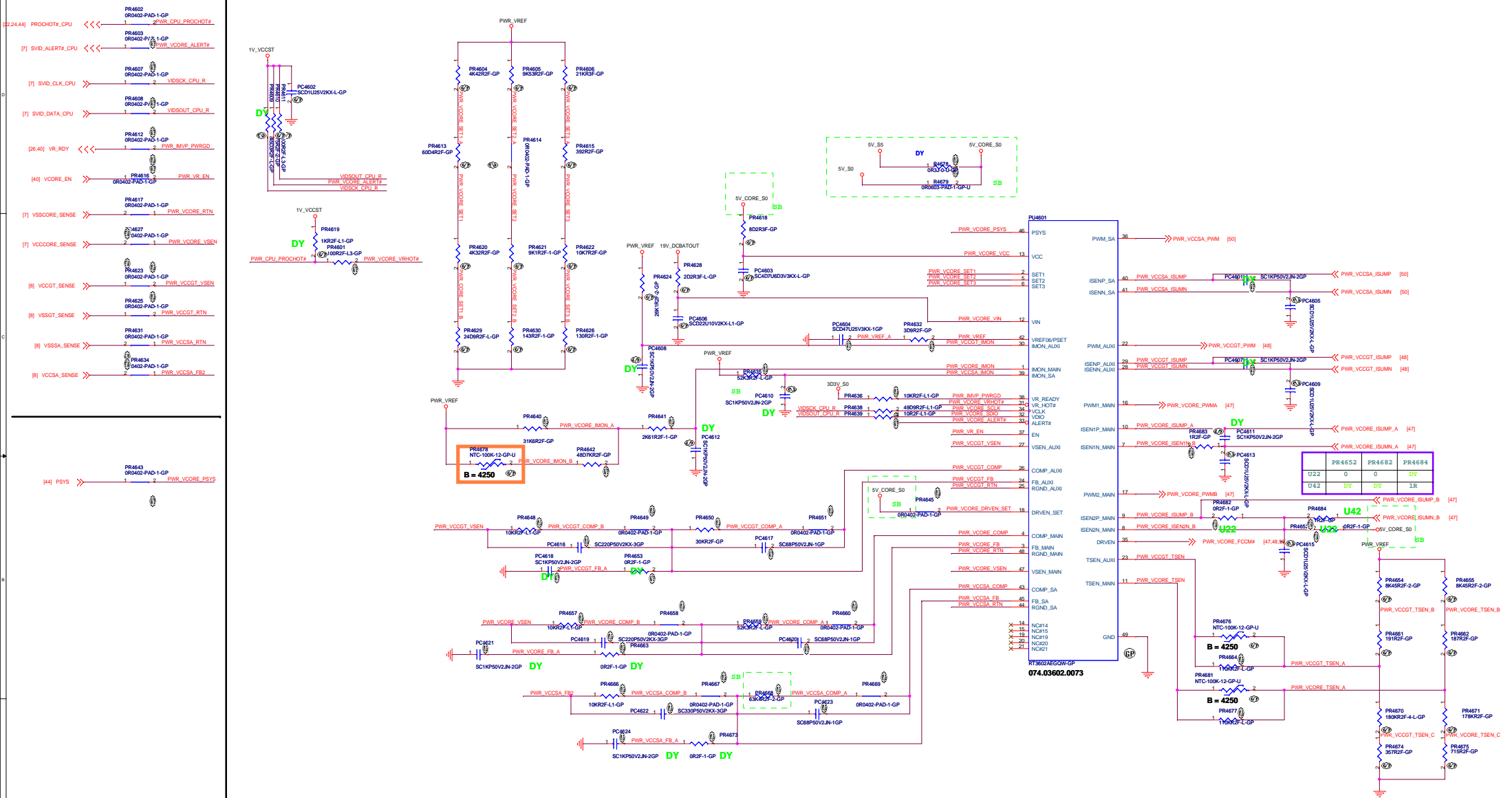


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File	<b>RT6575D 5V/3D3V</b>	
Rev	Document Number	Rev
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## OFFPAGE

```
Main Func = CPU_CORE
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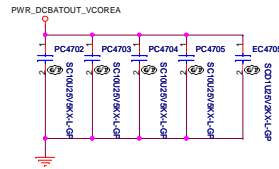
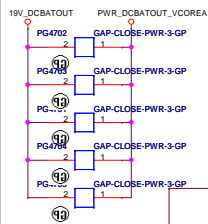


**E**

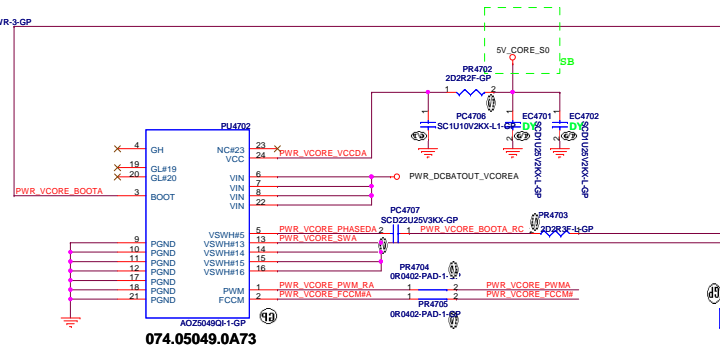
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Title			
Cover Page			
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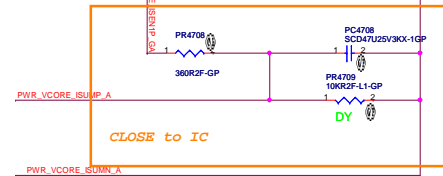
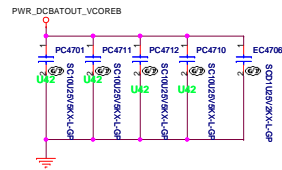
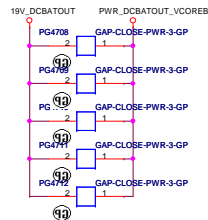
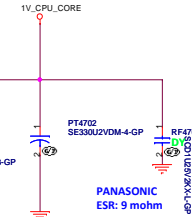
19V\_DCBATOUT      PWR\_DCBATOUT\_VCOREA



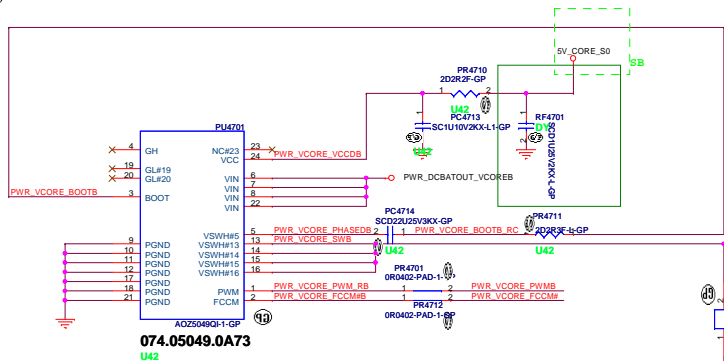
Confirm with EE  
22uF/0805 total 32pcs  
(78.22610.L2L)



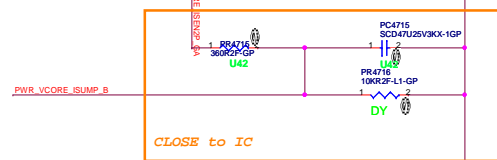
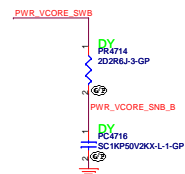
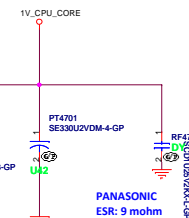
Cyntec. 6.8mm x7.6mmx3.0mm  
DCR: 0.9m Ohm+/-7%  
Idc : 37A , Isat : 41A  
PL4702



Confirm with EE  
22uF/0805 total 36pcs  
(78.22610.L2L)



Cyntec. 6.8mm x7.6mmx3.0mm  
DCR: 0.9m Ohm+/-7%  
Idc : 37A , Isat : 41A



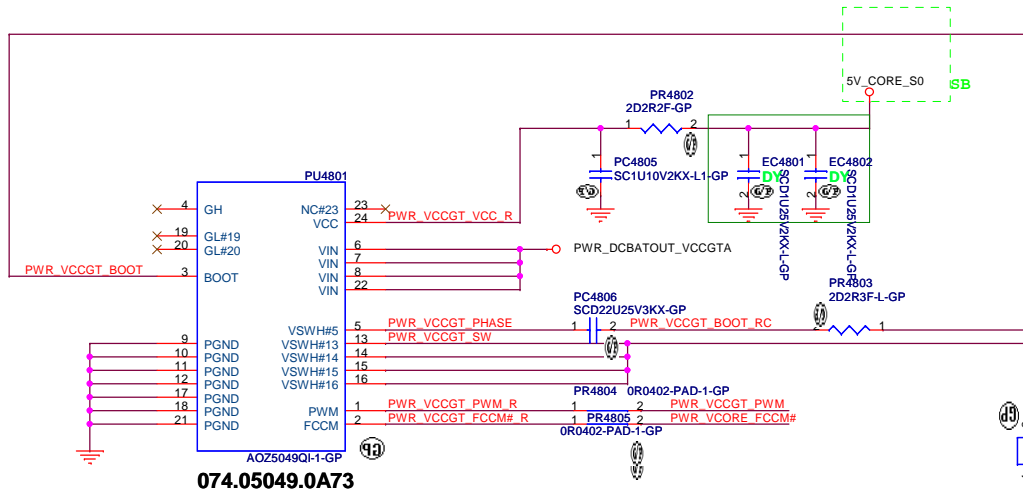
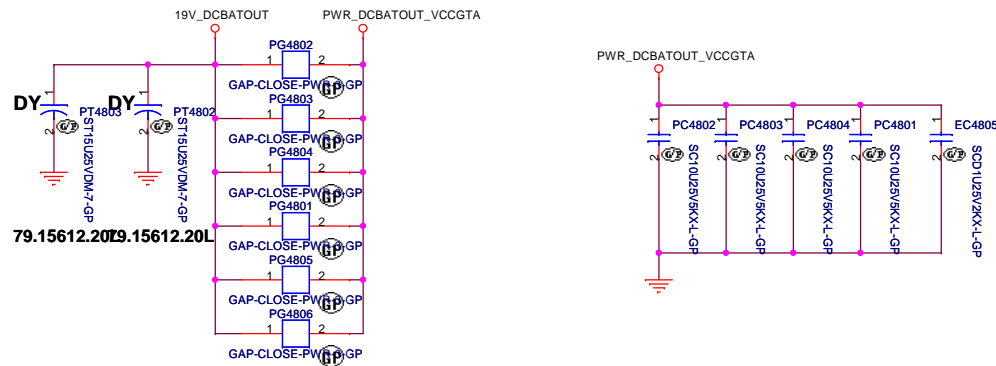
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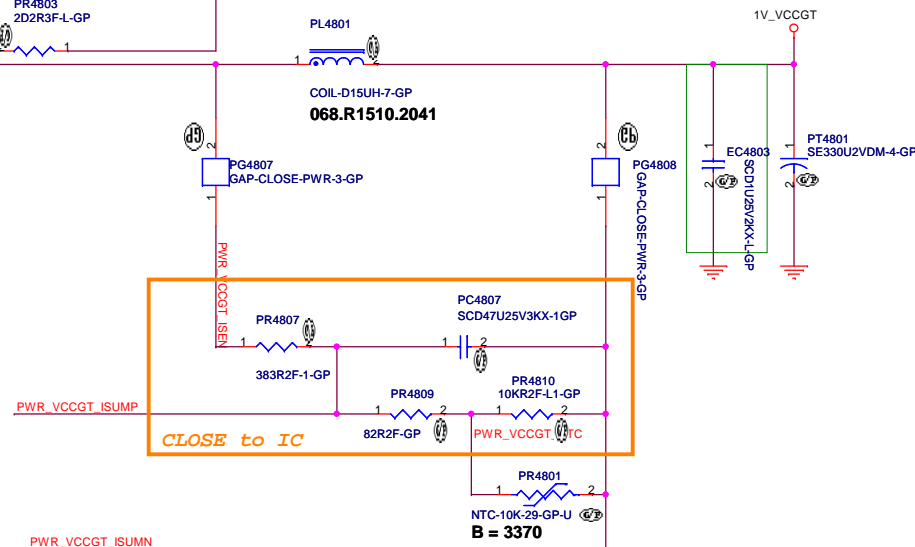
**Main Func = CPU\_CORE**



**SKL\_U42**  
Icc(max)=28A  
TDC=12A

Confirm with EE  
22uF/0805 total 26pcs  
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx3.0mm  
DCR: 0.9m Ohm+/-7%  
Idc : 37A , Isat : 41A



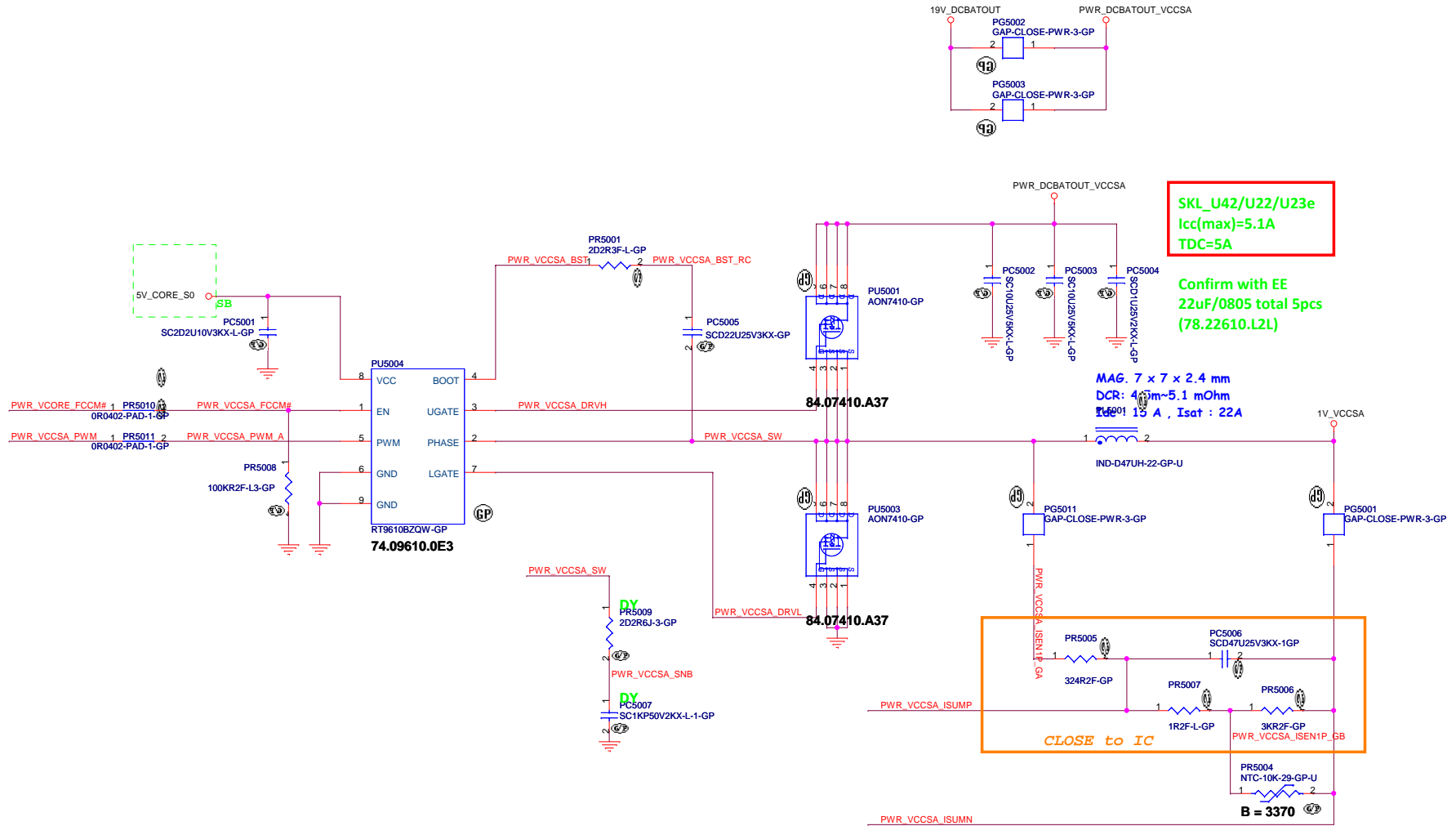
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Main Func = CPU\_CORE

[46,47,48] PWR\_VCORE\_FCM# >>>  
 [46] PWR\_VCCSA\_PWM >>>  
 [46] PWR\_VCCSA\_ISUMP <<<  
 [46] PWR\_VCCSA\_ISUMN <<<



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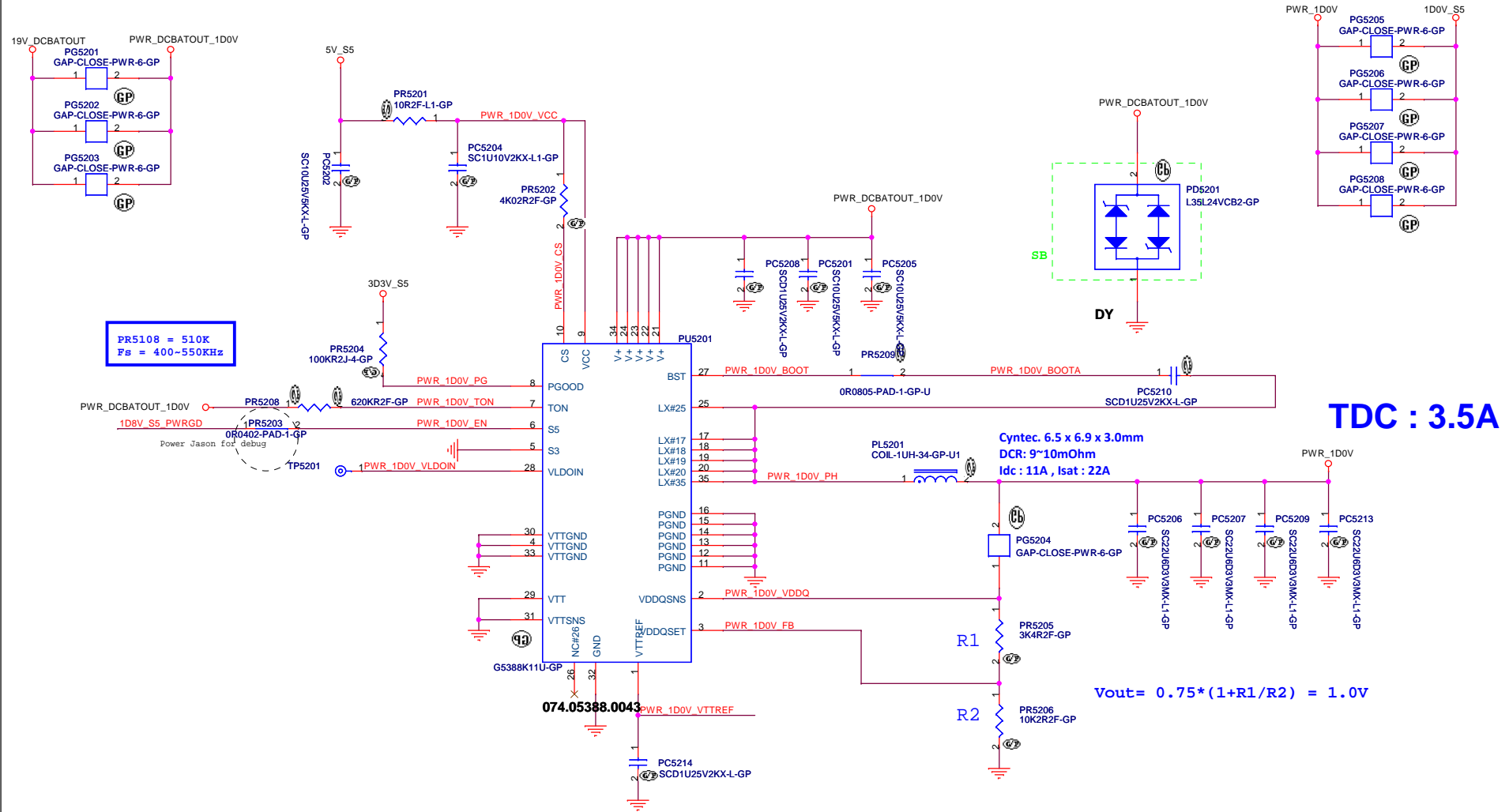
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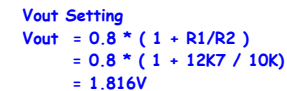
# 1D0V ENABLE CONTROL

[53] 1D8V\_S5\_PWRGD >>>



————>>1D8V\_S5\_PWRGD [52]

3V\_5V\_POK [20,45,73]



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# Main Func = LCD

20.K0809.040  
2nd = 20.K0678.040  
3rd = 020.K0160.0040

FOR G-SENSOR

[89] TOUCH\_DET#\_R <<<  
[89] TS\_S0 <<<  
[89] eDP\_TX\_CON\_P0 <<<  
[89] eDP\_TX\_CON\_N0 <<<  
[89] eDP\_TX\_CON\_P1 <<<  
[89] eDP\_TX\_CON\_N1 <<<  
[89] eDP\_AUX\_CON\_P <<<  
[89] eDP\_AUX\_CON\_N <<<  
[89] TOUCH\_INTR# <<<

[89] eDP\_HPDCON <<<  
[89] eDP\_BLECON <<<  
[89] eDP\_BLCCTRL\_CON <<<

[3] eDP\_VDDEN\_CPU >>>

[3] eDP\_AUX\_CPU\_P >>>  
[3] eDP\_AUX\_CPU\_N >>>

[3] eDP\_TX\_CPU\_P0 >>>  
[3] eDP\_TX\_CPU\_N0 >>>

[3] eDP\_TX\_CPU\_P1 >>>  
[3] eDP\_TX\_CPU\_N1 >>>  
[6] TOUCH\_S\_RST# >>>

[18,24,70,73,79] SML1\_DATA >>>  
[18,24,70,73,79] SML1\_CLK >>>

[6] TOUCH\_DET# >>>

[24] TOUCH\_EN >>>

[24] BLON\_OUT >>>

[3] eDP\_HPDCPU <<<

[3] eDP\_BLCCTRL\_CPU >>>

[15] TS\_USB20\_P <<<

[15] TS\_USB20\_N <<<

[6,24] TS\_I2C0\_SDA\_CON <<<

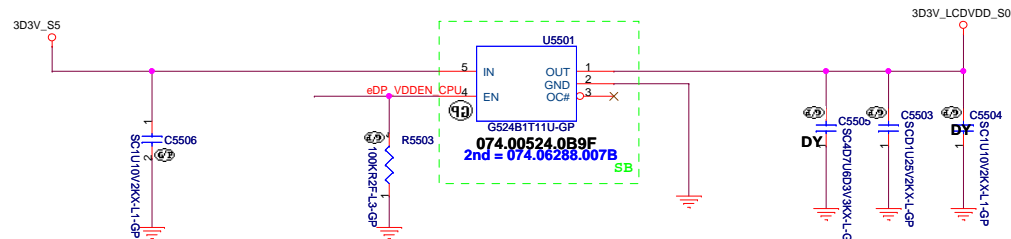
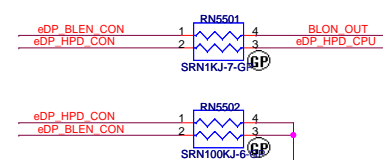
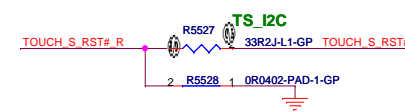
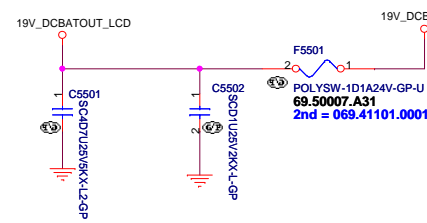
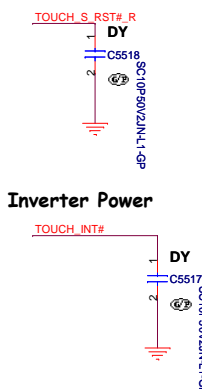
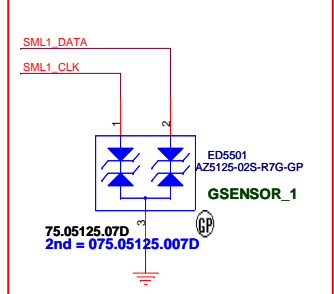
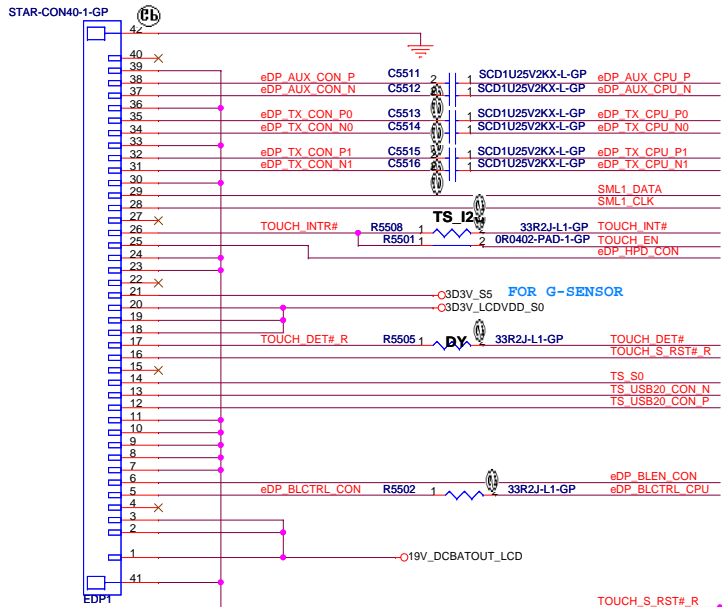
[6,24] TS\_I2C0\_SCL\_CON <<<

[22] TOUCH\_INT# <<<

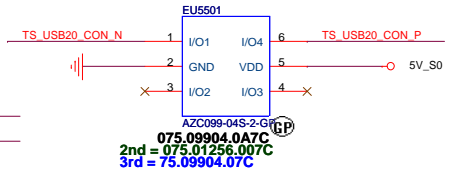
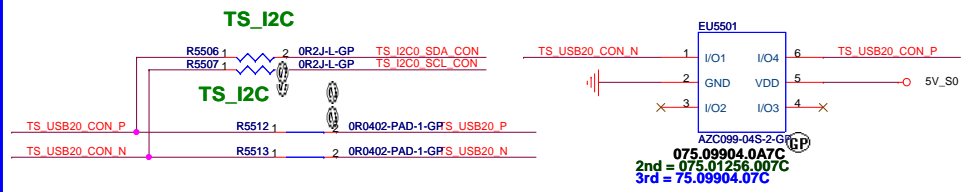
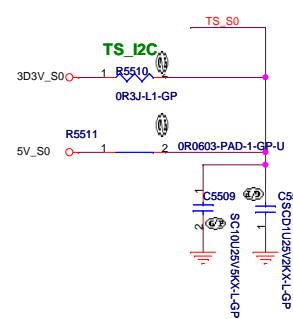
[89] TS\_USB20\_CON\_N <<<

[89] TS\_USB20\_CON\_P <<<

[89] TOUCH\_S\_RST#\_R <<<



## Touch panel Power

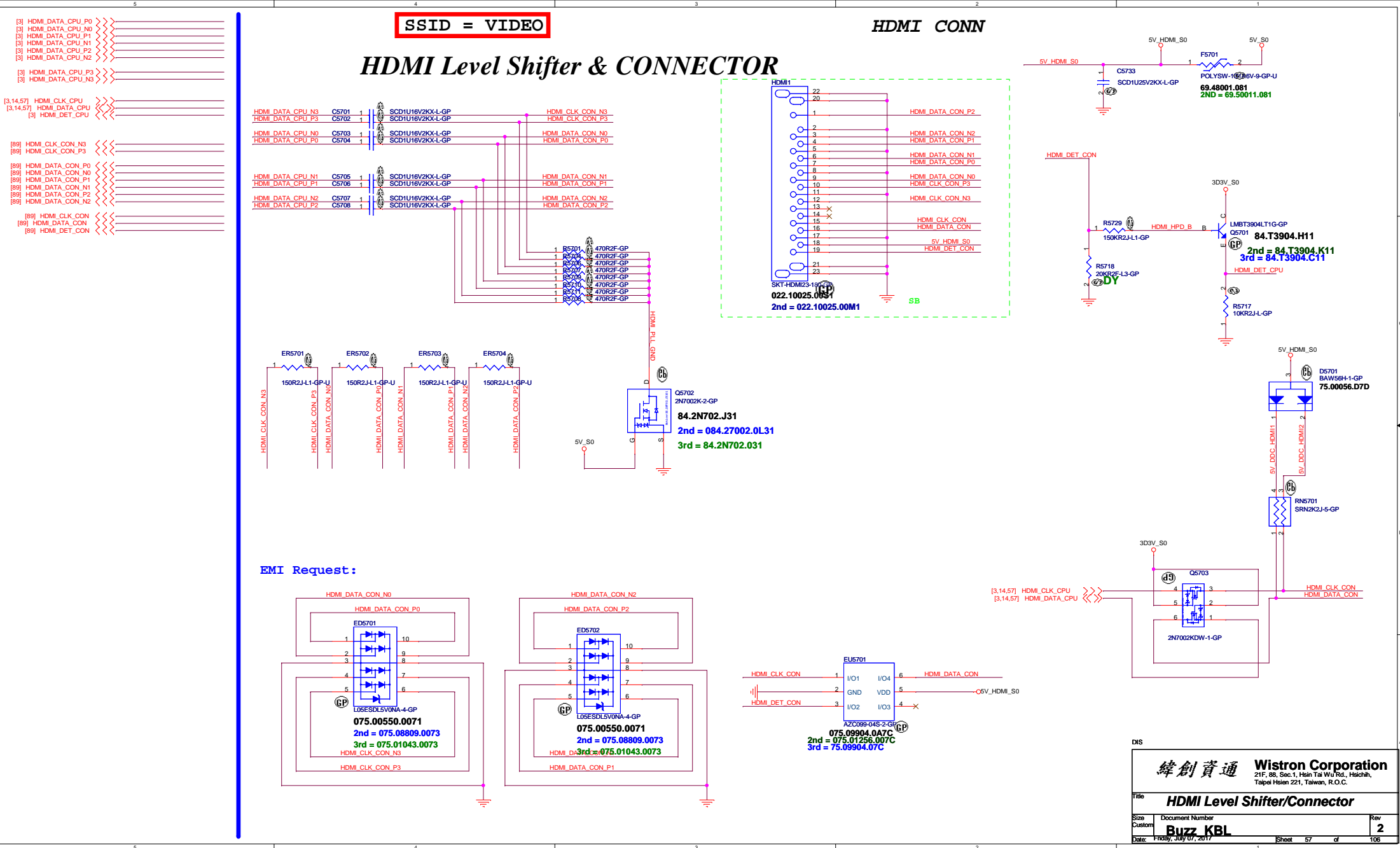


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Title LCD CONN			
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Title			
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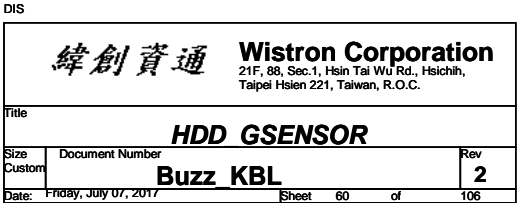
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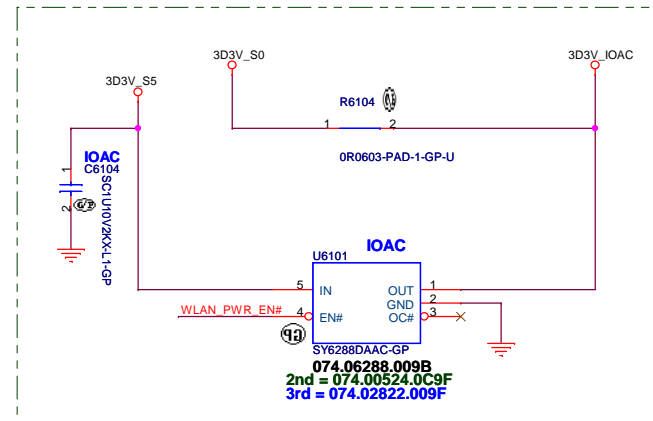
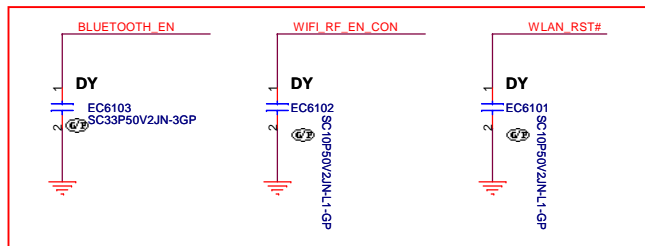
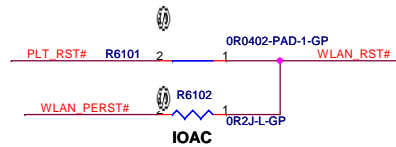
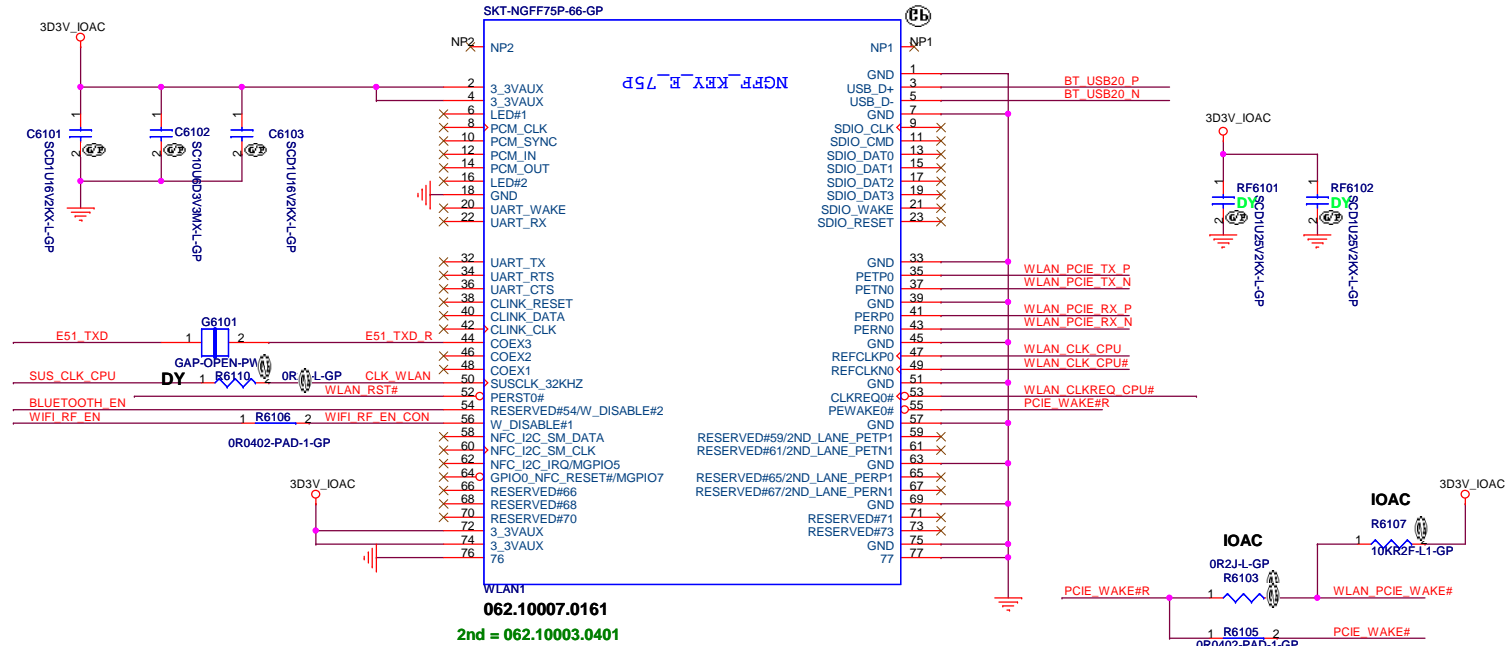
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SSID = SATA



**SSID = Wireless**



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Title	<b>Mini Card-WLAN</b>
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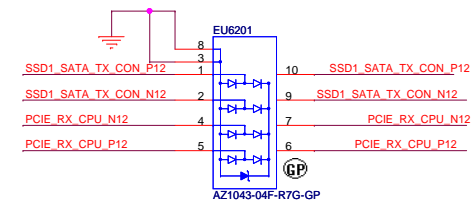
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### ***Mini Card Connector(mSATA)***




PCN-LP Details		PCnE Controller #1				PCnE Controller #2				PCnE Controller #3				
Flex I/O Lane #		5	6	7	8	5	6	7	8	12	13	14	15	16
PCnE Lane #		1	2	3	4	5	10	11	8	9	10	11	12	
Base-U	1x4	SP-1				SP-5				SP-9				
	2x2	SP-1		SP-3		SP-5				SP-9			SP-11	
	3x2/2x3	SP-1	SP-3	SP-4		SP-5				SP-9	SP-11	SP-12		
	2x3/1x2	SP-4	SP-3	SP-1			SP-5			SP-12	SP-11		SP-9	
	3x2	SP-1	SP-2	SP-3	SP-4	SP-5				SP-9	SP-10	SP-11	SP-12	
	1x6	SP-1				SP-5				SP-9				
Premium-U	1x4	SP-1				SP-5				SP-9				
	2x2	SP-1		SP-3		SP-5		SP-7		SP-9			SP-11	
	3x2/2x3	SP-1	SP-3	SP-4		SP-5	SP-7	SP-8		SP-9	SP-11	SP-12		
	2x3/1x2	SP-4	SP-3	SP-1		SP-5	SP-7			SP-12	SP-11		SP-9	
	3x2	SP-1	SP-2	SP-3	SP-4	SP-5	SP-6	SP-7	SP-8	SP-9	SP-10	SP-11	SP-12	
	1x6	SP-1				SP-5				SP-9				
Premium-Y	1x4	SP-1				SP-5				SP-9				
	2x2	SP-1		SP-3		SP-5		SP-7		SP-9				
	3x2/2x3	SP-1	SP-3	SP-4		SP-5	SP-7	SP-8		SP-9				
	2x3/1x2	SP-4	SP-3	SP-1		SP-5	SP-7						SP-9	
	3x2	SP-1	SP-2	SP-3	SP-4	SP-5	SP-6	SP-7	SP-8	SP-9	SP-10			
	1x6	SP-1	SP-2	SP-3	SP-4	SP-5	SP-6	SP-7	SP-8	SP-9	SP-10			

\*\* Native: Internal Pull-Up (15k-40k) when function.

State #	Module Configuration Decodes				Module Type and Main Host Interface <sup>1</sup>	Port Configuration <sup>2</sup>
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

- Notes:**
1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
  2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
  3. Design Constraint: For PCIe\* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
  4. Design Constraint: For PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
  5. Design Constraints, Required: Refer to Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
  6. Design Constraint: For PCIe\* lane that needs to support either PCIe\* Gen2 devices or PCIe\* Gen3 devices, follow the PCIe\* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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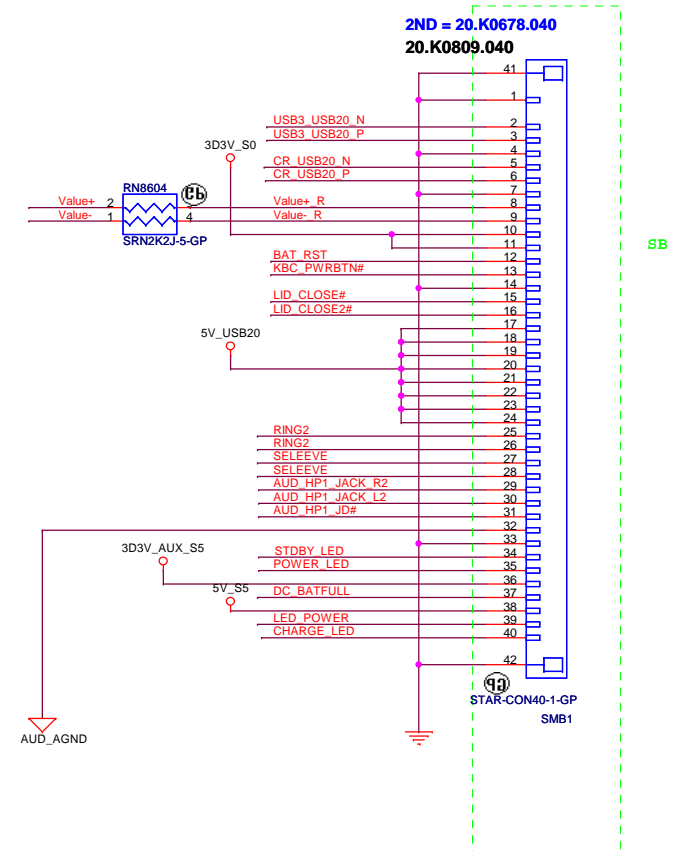
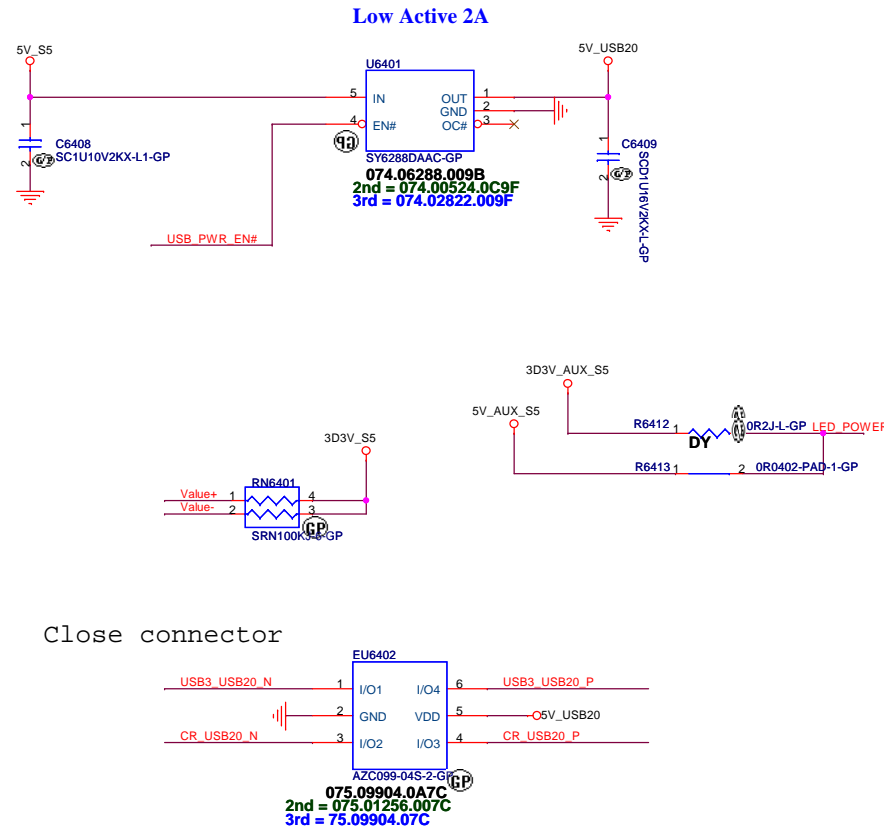
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```
SSID = User.Interface
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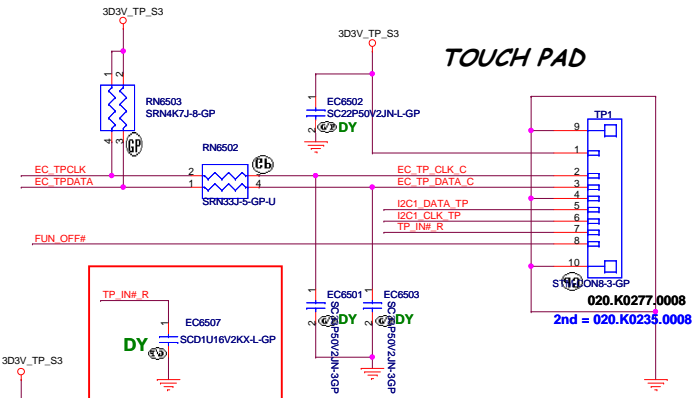
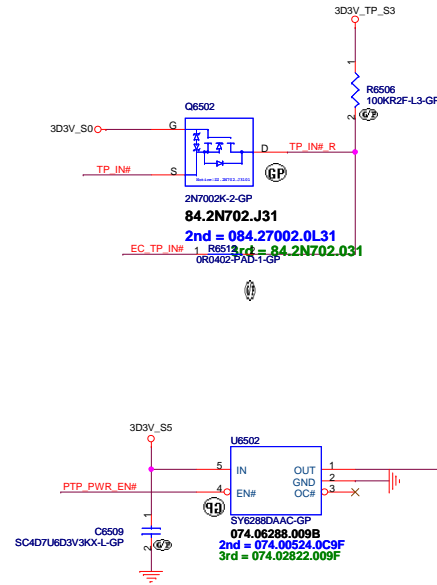
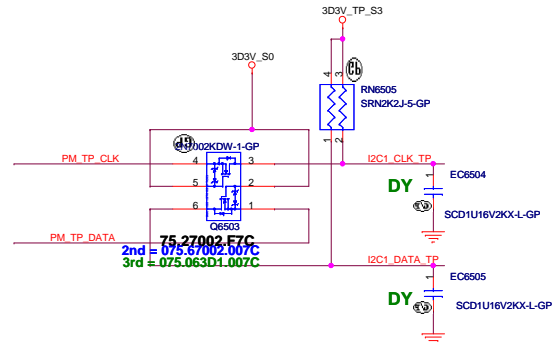
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Title	<b>LED Bard/Power Button</b>
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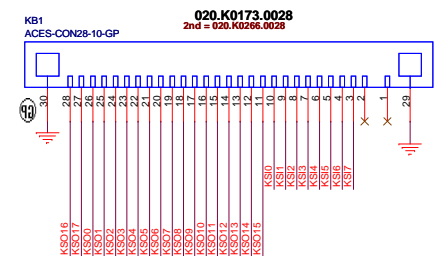
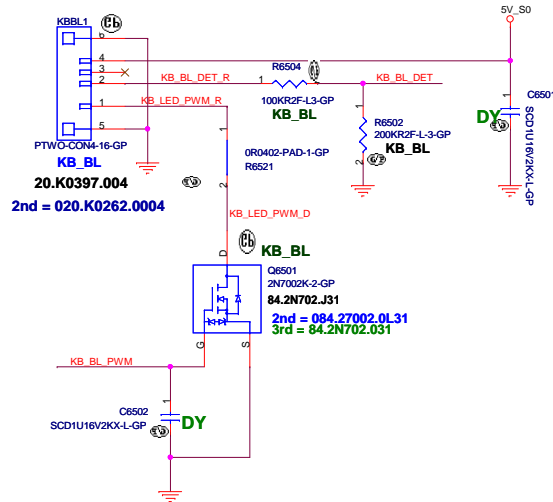
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SSID = KBC

[24,89] KSI[0..7] >>>   
 [24,89] KSO[0..17] <<<   
 [24] EC\_TPCLK >>>   
 [24] EC\_TPDATA >>>   
 [24,89] FUN\_OFF# >>>   
 [89] EC\_TP\_CLK\_C >>>   
 [89] EC\_TP\_DATA\_C >>>   
 [89] I2C1\_CLK\_TP >>>   
 [89] I2C1\_CLK\_TP >>>   
 [89] TP\_IN#\_R >>>   
 [24] PTP\_PWR\_EN# >>>   
 [22] TP\_IN# <<<   
 [24] EC\_TP\_IN# <<<   
 [6] PM\_TP\_CLK <<<   
 [6] PM\_TP\_DATA <<<   
 [24] KB\_BL\_PWM >>>   
 [24] KB\_BL\_DET <<<   
 [89] KB\_LED\_PWM >>>   
 [89] KB\_BL\_DET\_R <<< 



## Internal KeyBoard Connector



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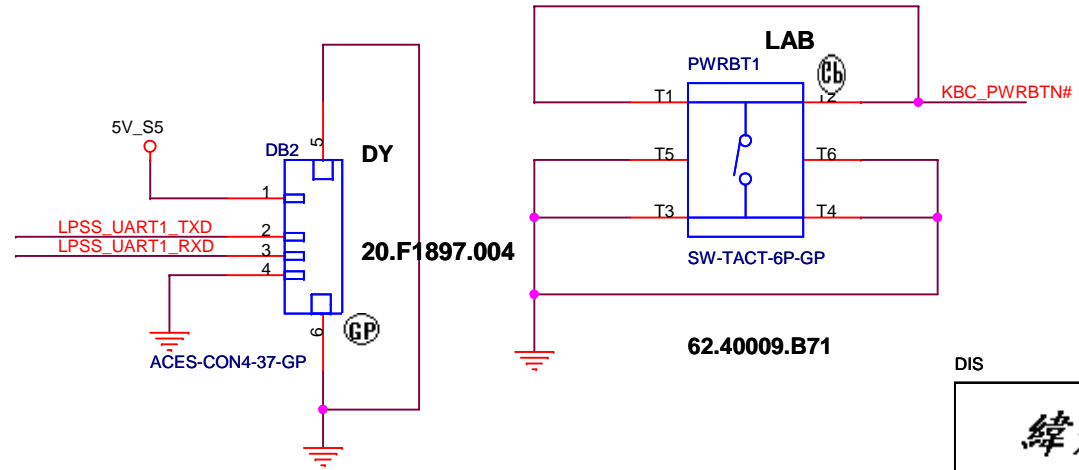
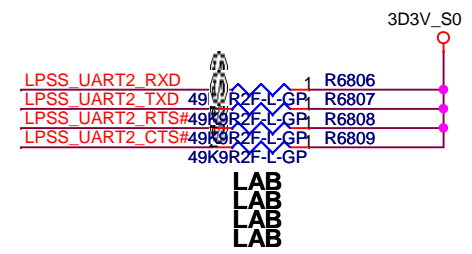
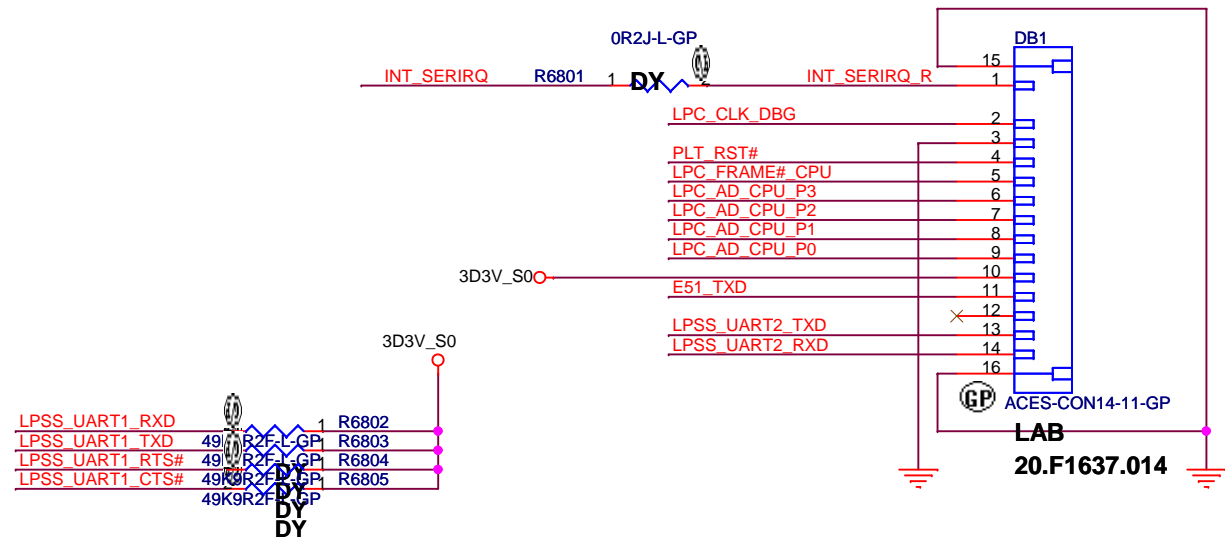
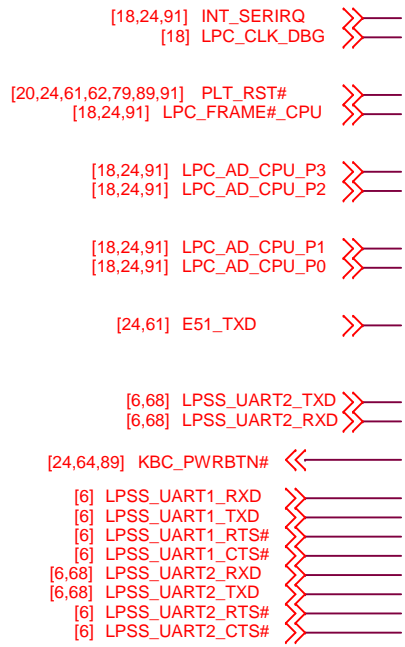
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**2**

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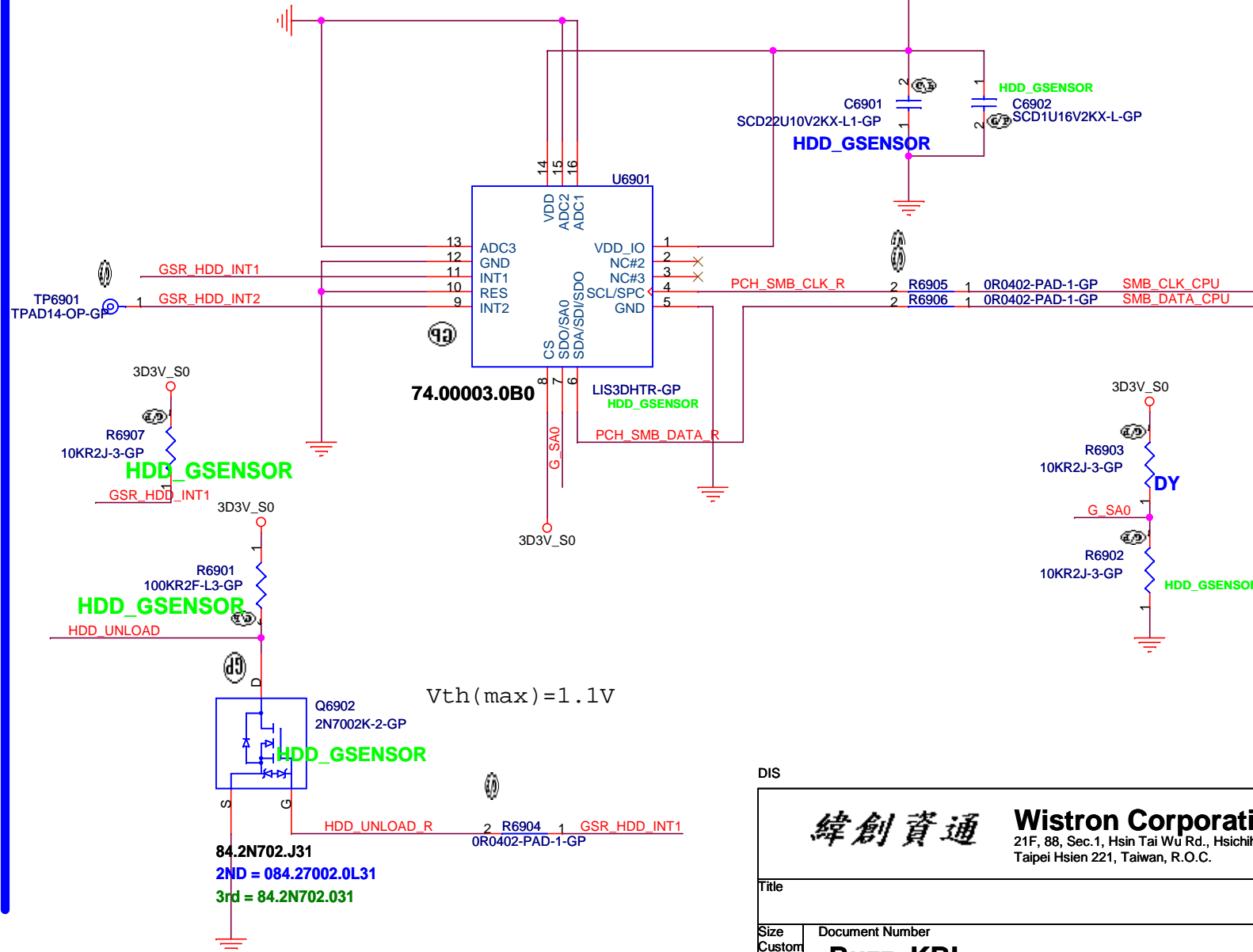
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Title Dubug connector		
Size A4	Document Number Buzz KBL	Rev 2
Date: Friday, July 07, 2017		Sheet 68 of 106

[18] SMB\_CLK\_CPU <<<  
[18] SMB\_DATA\_CPU <<<

[22] GSR\_HDD\_INT1 <<<

[60] HDD\_UNLOAD <<<



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Size Custom	Document Number <b>Buzz KBL</b>	Rev <b>2</b>	
Date: Friday, July 07, 2017	Sheet 69 of 106	Date:	

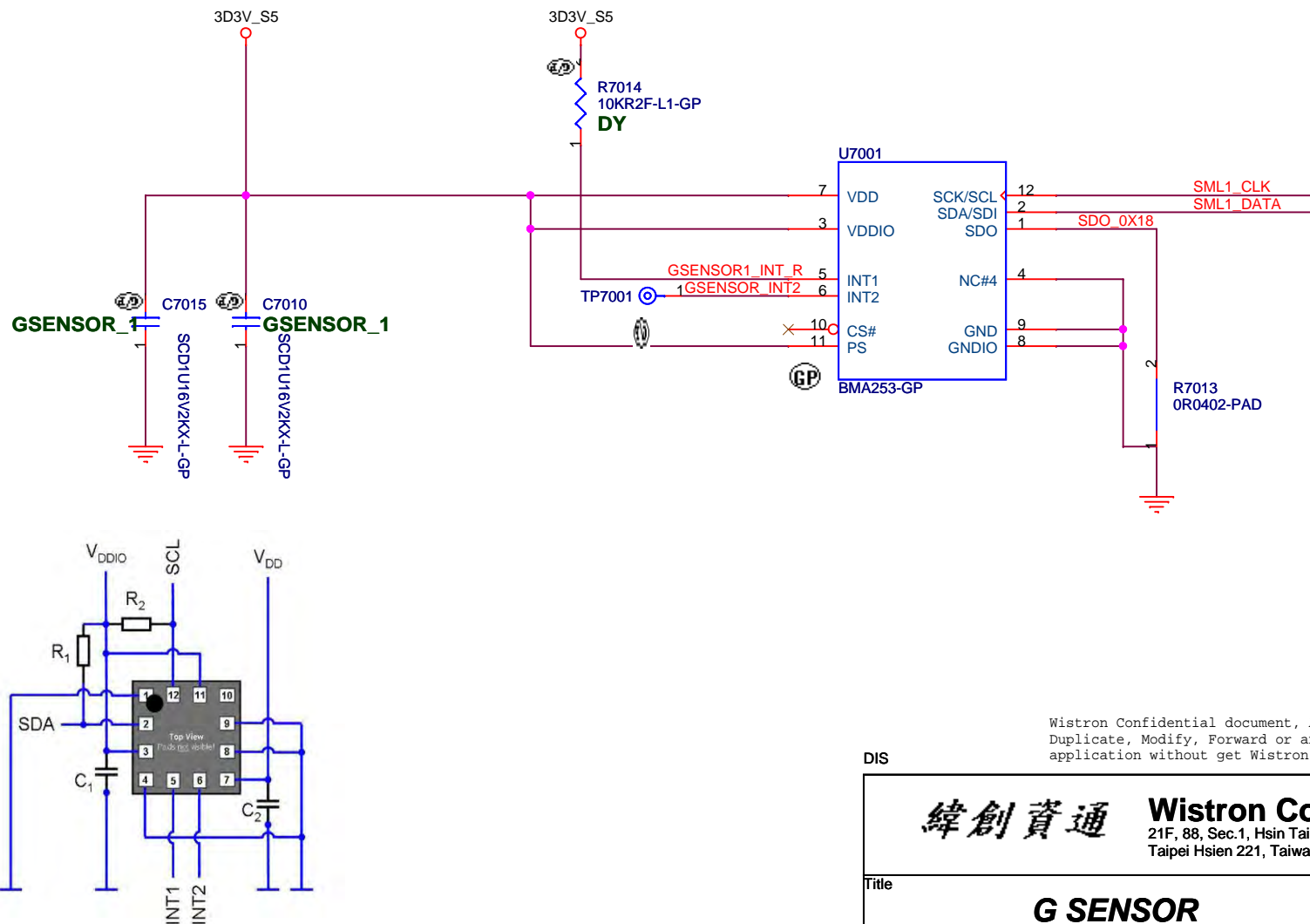
```
SSID = User.Interface
```

## G Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

The default I<sup>2</sup>C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V<sub>DDIO</sub>'.



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## ***G SENSOR***

Size	Document Number
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**Custom**

## Buzz KBL

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2

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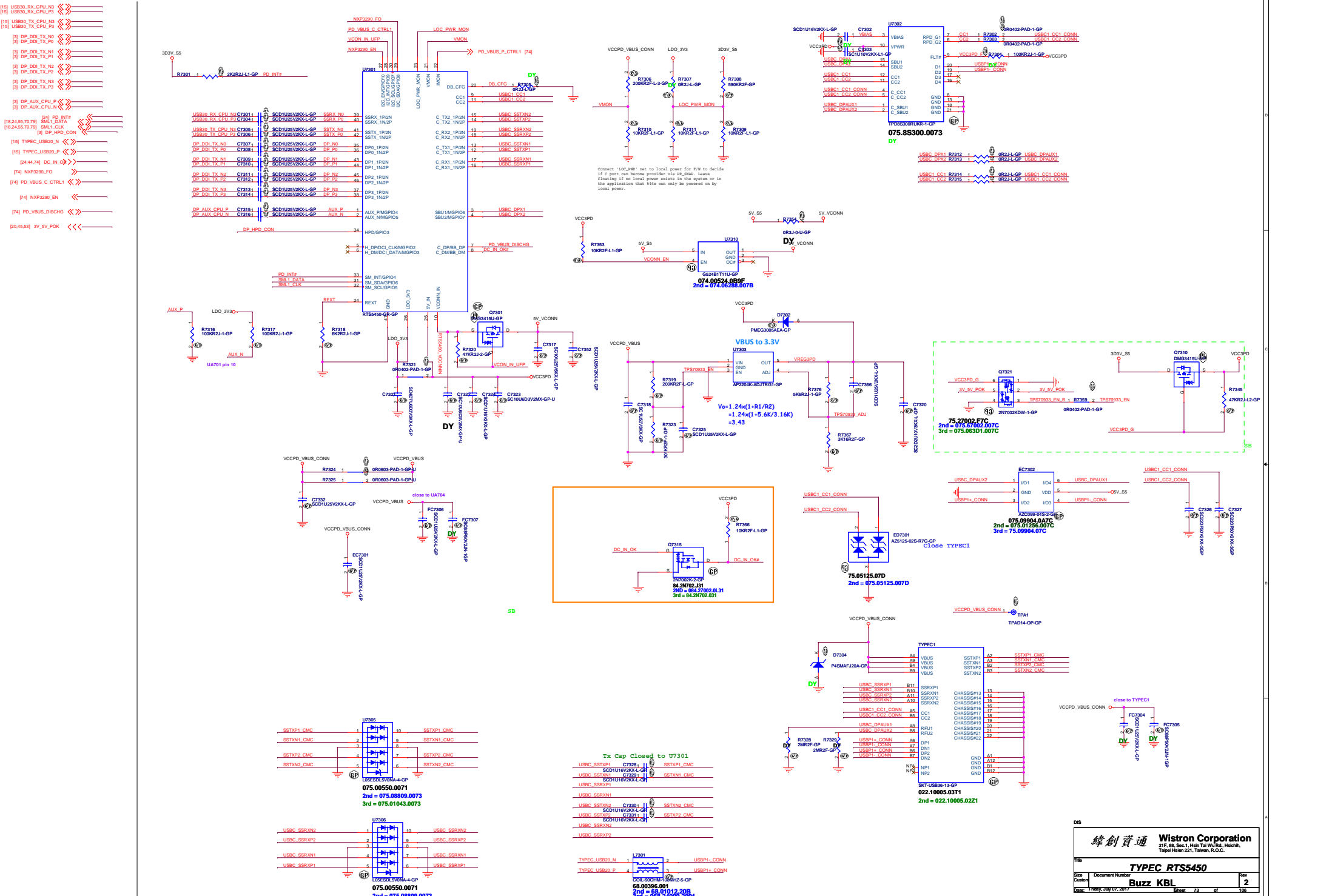


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Title					
Size A4	Document Number <b>Buzz KBL</b>				Rev <b>2</b>
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Type	
Document Number	
TypeC RTSS450	
Rev	
2	
Date	Friday, 20/07/2017
Drawn	73
of	108

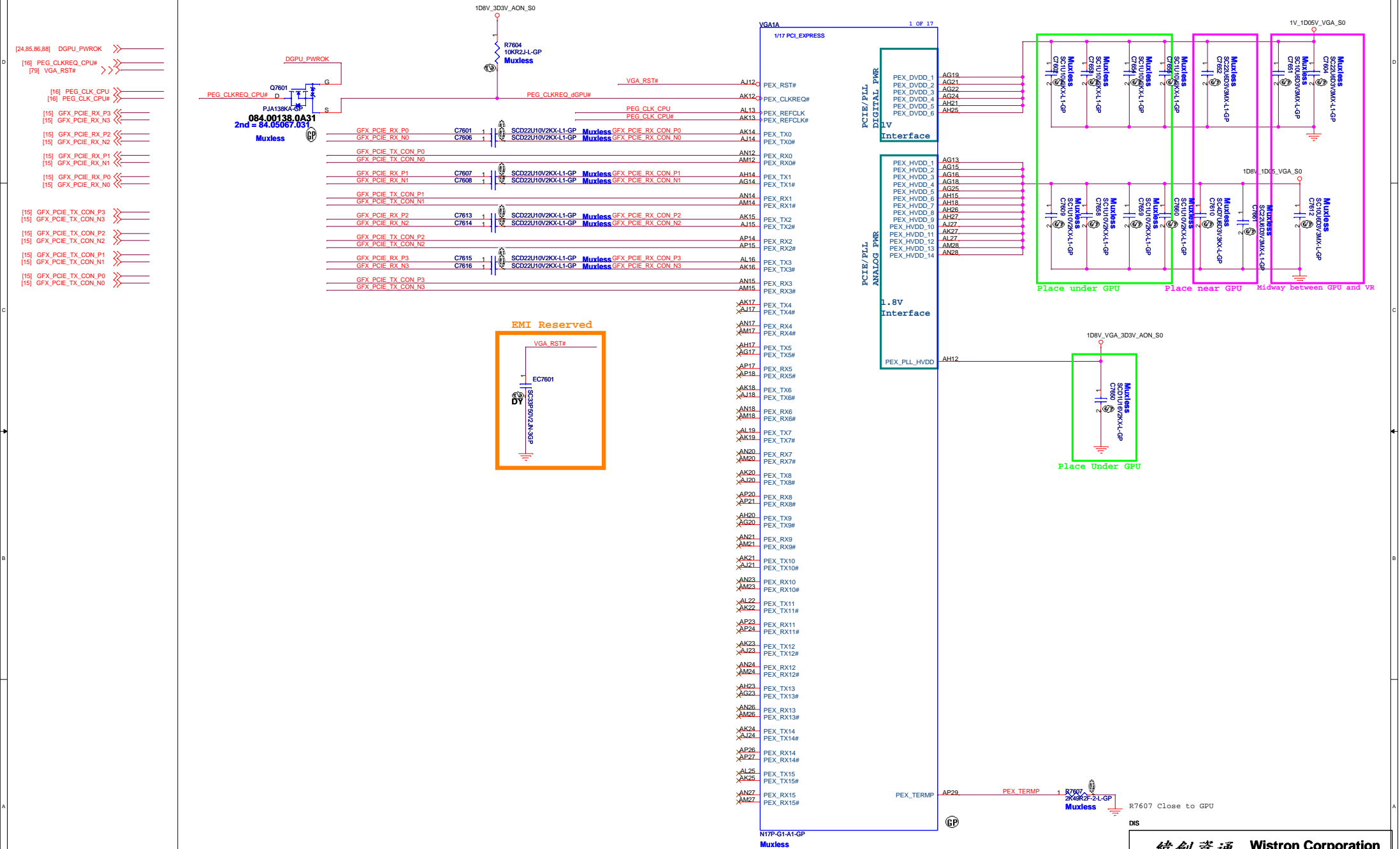


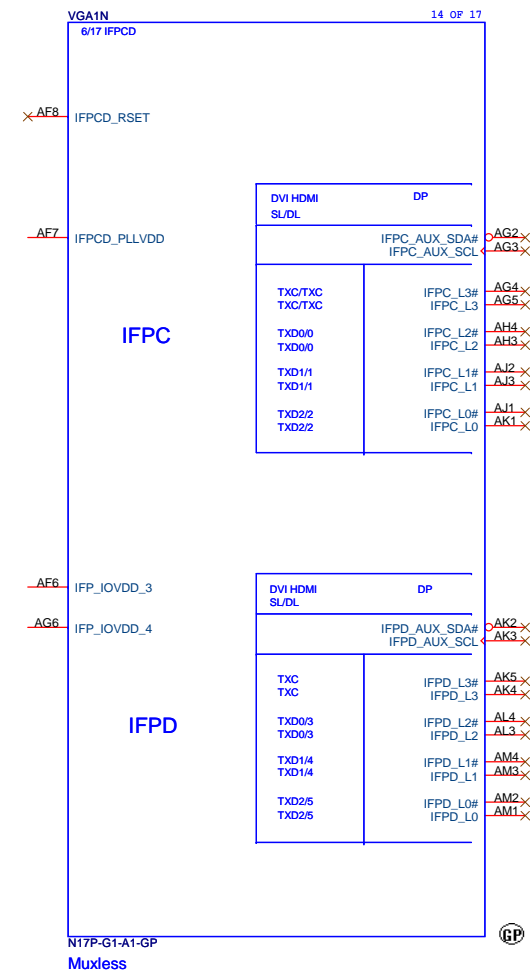
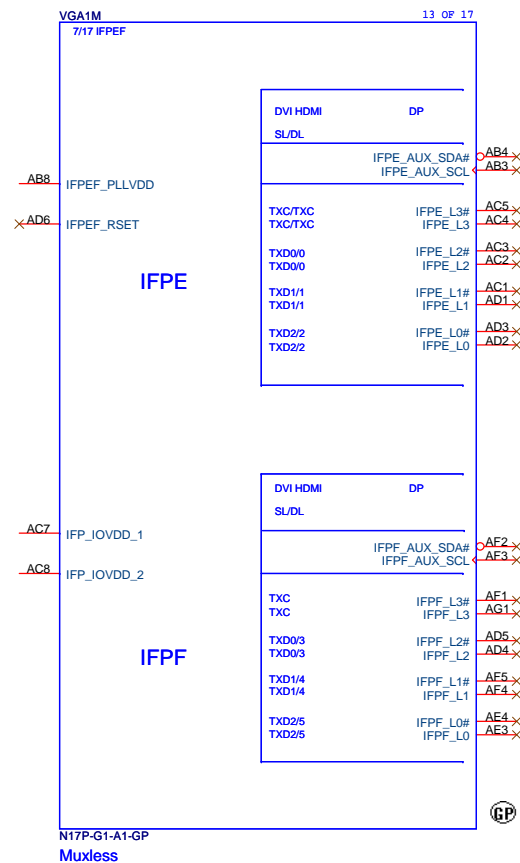
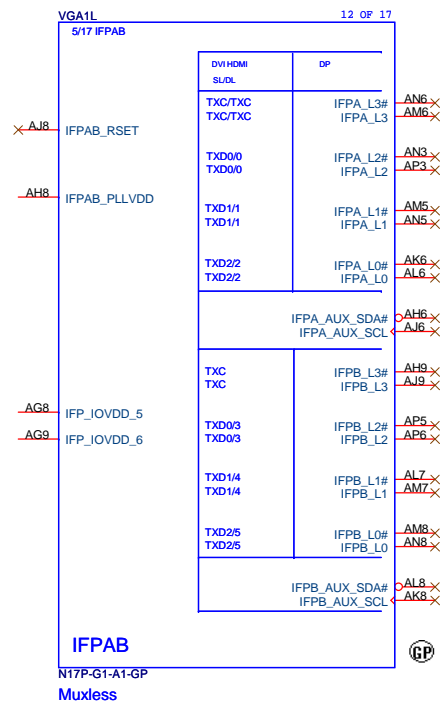


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Title		
GPU (VRAM I/F)		
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STRAP0	STRAP1	STRAP2	Vendor PN
L	L	L	Samsung K4G80325FB-NC28
H	L	L	Micron MT51J256M32HF-70:A
L	H	L	Hynix H5GC8H24MJR-R0C

Assembly Number	Approved Material Specification	Part Number	Material	Manufacturer Part Number	Dis posi tion	Material Status	Material Brand Code	Date Code	Unit Type	Notes
1-Gb	2548A.02	1.33V and 1.5V	Memcon	MT6125A48-10C-18	7-die	0-1	7-Gram	N/A	Full	Product candidate
		1.33V	Hynix	HY5GC1040AB-RDC	6-die	0-2	7-Gram	N/A	Full	Product candidate
		1.5V	Hynix	HY5GC1040AB-RDC	6-die	0-2	7-Gram	N/A	Full	Product candidate
4-Gb	3278A.02	1.33V and 1.5V	Hynix	HY5GC1040AB-RDC	6-die	0-6	7-Gram	N/A	Full	Product candidate
		1.33V	Hynix	HY5GC1040AB-RDC	6-die	0-6	7-Gram	N/A	Full	Product candidate
		1.5V	Hynix	HY5GC1040AB-RDC	6-die	0-6	7-Gram	N/A	Full	Product candidate
		1.33V	Memcon	MT6125A48-10C-18	7-die	0-6	7-Gram	N/A	Full	Product candidate
		1.5V	Memcon	MT6125A48-10C-18	7-die	0-6	7-Gram	N/A	Full	Product candidate

Strap Pins and Pins			RANCO Setting Number		Strap Pins and Pins			RANCO Setting Number	
STRAP1	STRAP2	STRAP3	(See Manual RVI for the memory settings corresponding to these numbers)		STRAP2	STRAP1	STRAP0	(See Manual RVI for the memory settings corresponding to these numbers)	
			2 (000002)		N	N	N	14 (000014)	
			3 (000003)		N	N	N	15 (000015)	
			4 (000004)		N	N	N	16 (000016)	
			5 (000005)		N	N	N	17 (000017)	
			6 (000006)		N	N	N	18 (000018)	
			7 (000007)		N	N	N	19 (000019)	
			8 (000008)		N	N	N	20 (000020)	
			9 (000009)		N	N	N	21 (000021)	
			10 (000010)		N	N	N	22 (000022)	
			11 (000011)		N	N	N	23 (000023)	
			12 (000012)		N	N	N	24 (000024)	
			13 (000013)		N	N	N	25 (000025)	

STRAP3	STRAP4	STRAP5	Function
L	L	L	as below picture

RCM_SLK	RCM_SI	RCM_SO	Function
M(0.9V)	L	L	as below picture

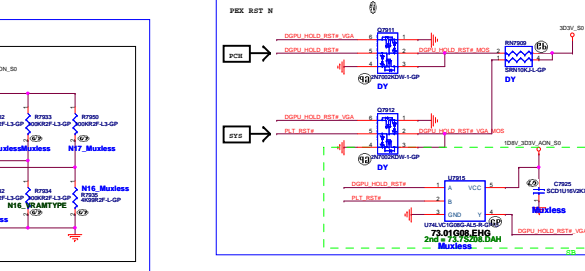
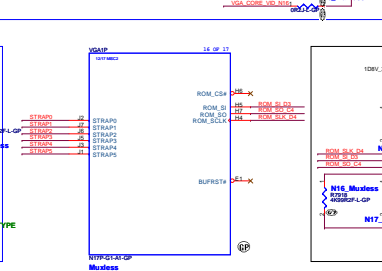
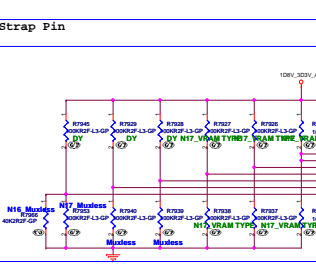
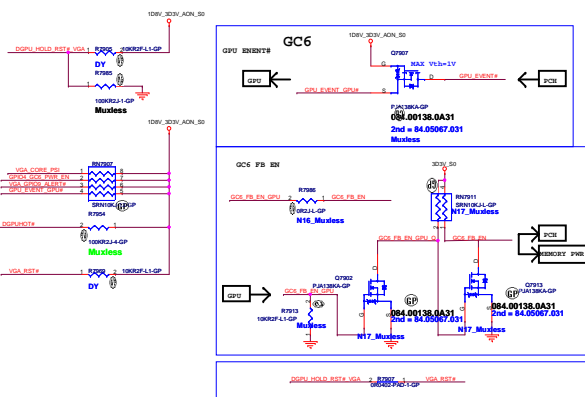
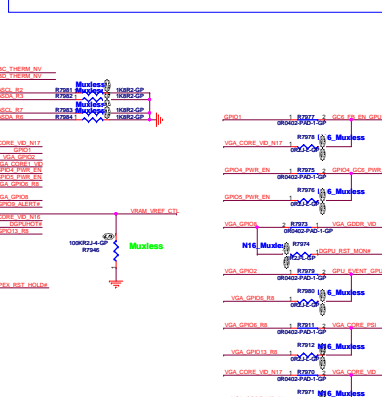
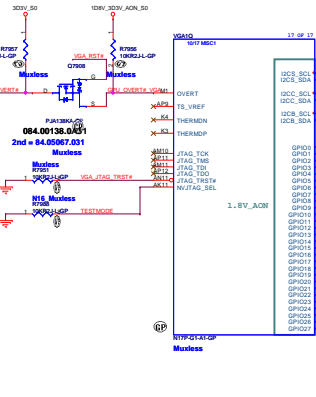
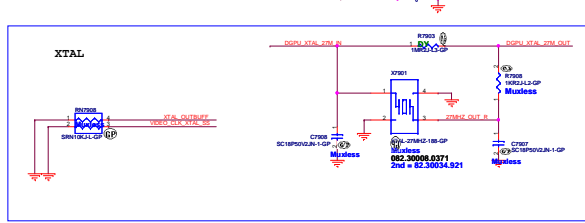
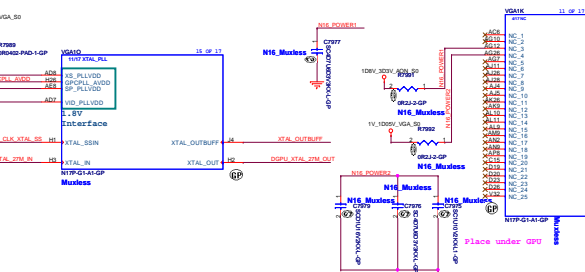
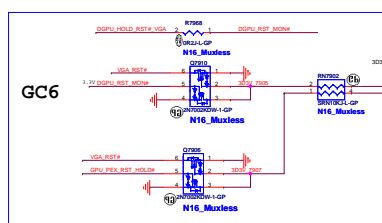
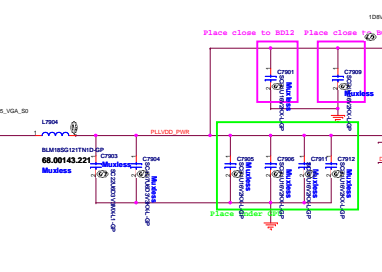
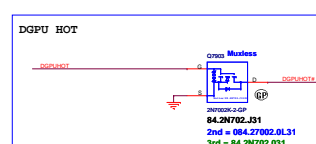
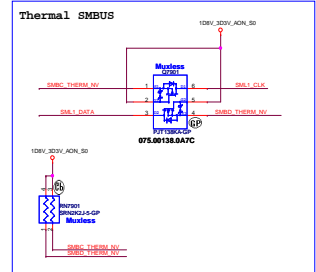
Row Index	Strap Pins <small>See Note</small>			Resulting SORA_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR1_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	DISABLED
13	L	H	L	ENABLED	ENABLED	DISABLED	ENABLED
12	L	H	H	ENABLED	ENABLED	DISABLED	DISABLED
11	H	L	L	ENABLED	DISABLED	ENABLED	ENABLED
10	H	L	H	ENABLED	DISABLED	ENABLED	DISABLED
9	H	H	L	ENABLED	DISABLED	DISABLED	DISABLED
8	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

GENES Device	STRAP0		STRAP1		STRAP2		Vendor FW			
	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	STRAP5	STRAP6	STRAP7	STRAP8	Vendor FW
Shanghai K46803259P-DC28	NA	100K	NA	100K	NA	100K	L	L	L	Samsung K46803259P-DC28
Micron MTSL1256M328P-70: A	NA	100K	NA	100K	NA	100K	H	L	L	Micron MTSL1256M328P-70: A
Hylix H50C882387P-ROC	NA	100K	NA	100K	NA	100K	L	H	L	Hylix H50C882387P-ROC

Function	STRAP3		STRAP4		STRAP5	
	R7928	R7939	R7929	R7940	R7945	R7953
0000 ALT ADDR DEVID DEL PCI2 CPU VGA DEVICE	NA	100K	NA	100K	NA	100K

STRAP3	STRAP4	STRAP5	Function
L	L	L	as Table 5.4

Function	ROM_SLK_D5		ROM_SI_D4		ROM_SO_C5	
	R7903	R7933	R7934	R7935	R7951	R7939
<b>SOREX_EXPOSED</b>	100K	100K	NA	100K	NA	100K



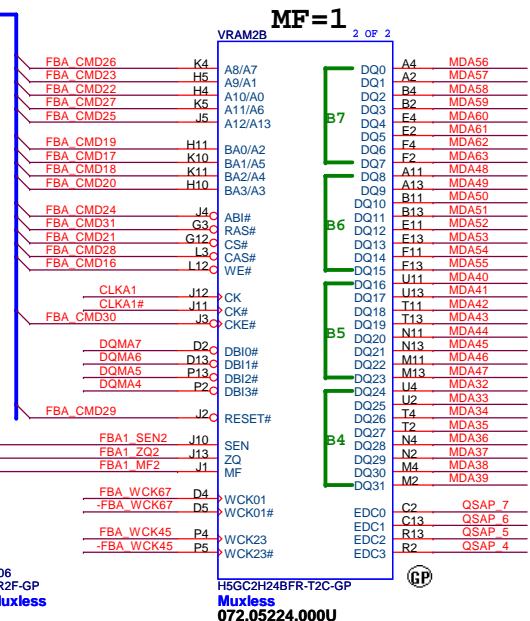
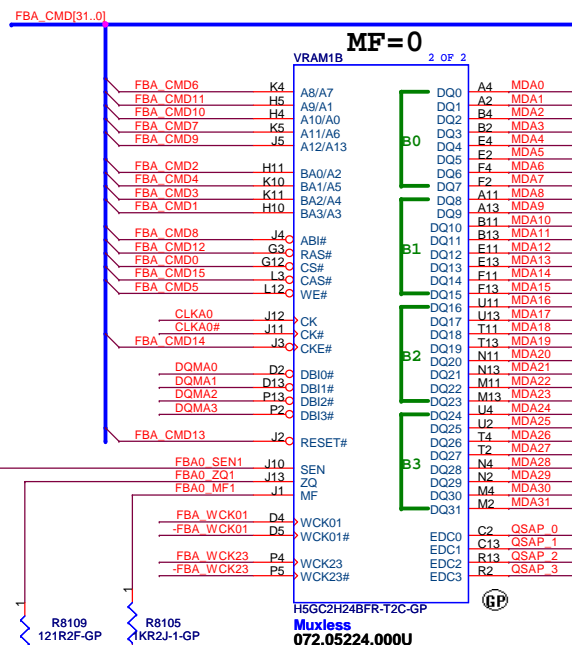
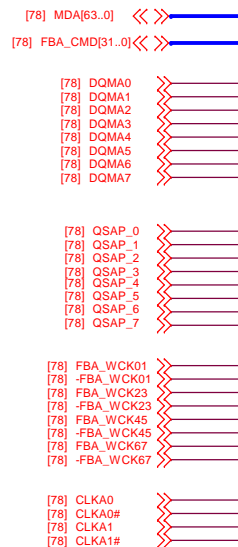
## N16P VRAM MATRIX

[illegible]

Hynix 4G/Samsung 2G	4.99Kohm	64.49915.6DL
	10Kohm	64.10025.L0L
Samsung 4G	15Kohm	64.15025.6DL
	20Kohm	64.20025.6DL
Hynix 2G	24.9Kohm	64.24925.6DL
	30.1Kohm	64.30125.6DL
	34.8Kohm	64.34825.6DL
	45Kohm	64.45325.6DL







GDDR5 Data Mapping							
BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQ50)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DB4)	DBI1	DBI2 (DB5)	DBI2	DBI1 (DB6)	DBI3	DBI0 (DB7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)
GDDR5 CLK Mapping							
WCK01	WCK23 (WCK45)			WCK23	WCK01 (WCK67)		
WCK01#	WCK23# (WCK45#)			WCK23#	WCK01# (WCK67#)		
CK	CK						
CK#	CK#						
Others							
MF	MF	SEN	SEN				
ZQ	ZQ	RESET#	RESET#				

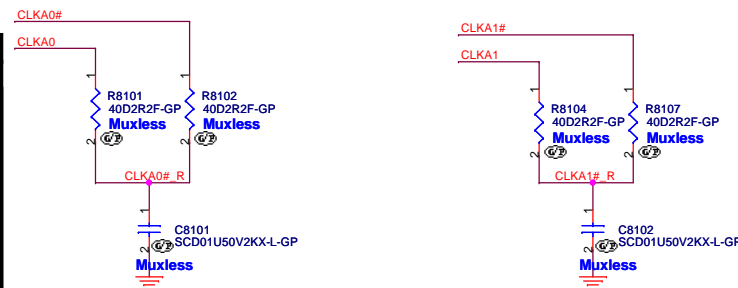


Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

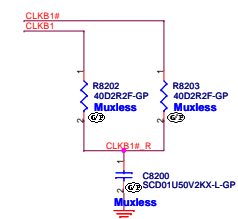
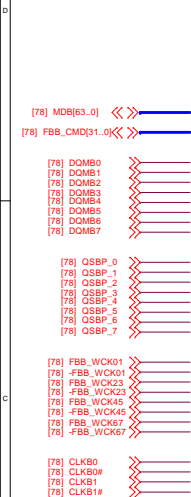
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

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Title		VRAM 1,2 (1/4)	
Size Custom	Document Number	Buzz_KBL	Rev 2
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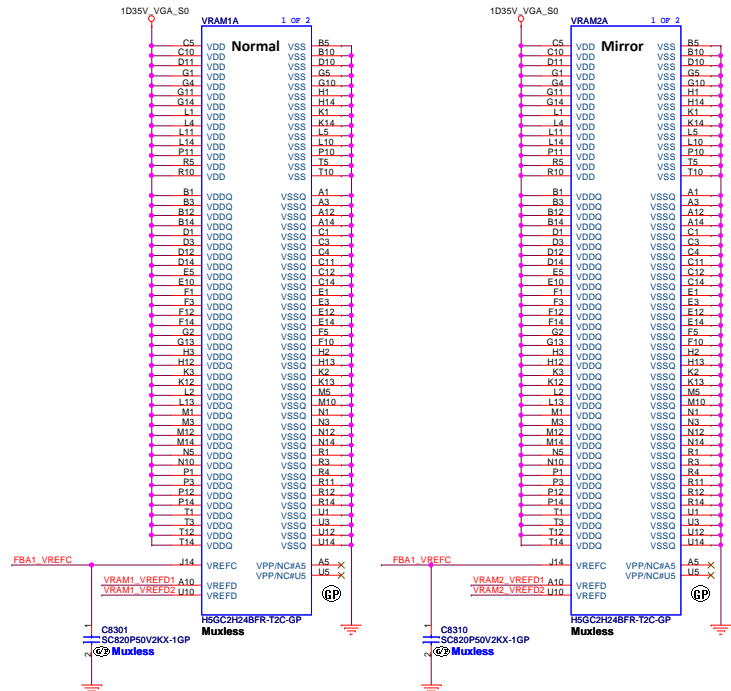


GDDR5 Data Mapping							
BYTE0 (BYTE4)		BYTE1 (BYTES)		BYTE2 (BYTES)		BYTE3 (BYTES)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ04)	DQ8	DQ16 (DQ04)	DQ16	DQ8 (DQ04)	DQ24	DQ0 (DQ04)
DQ1	DQ25 (DQ03)	DQ9	DQ17 (DQ01)	DQ17	DQ9 (DQ04)	DQ25	DQ1 (DQ03)
DQ2	DQ26 (DQ04)	DQ10	DQ18 (DQ02)	DQ18	DQ10 (DQ03)	DQ26	DQ2 (DQ04)
DQ3	DQ27 (DQ05)	DQ11	DQ19 (DQ03)	DQ19	DQ11 (DQ01)	DQ27	DQ3 (DQ05)
DQ4	DQ28 (DQ06)	DQ12	DQ20 (DQ04)	DQ20	DQ12 (DQ02)	DQ28	DQ4 (DQ06)
DQ5	DQ29 (DQ07)	DQ13	DQ21 (DQ05)	DQ21	DQ13 (DQ03)	DQ29	DQ5 (DQ07)
DQ6	DQ30 (DQ08)	DQ14	DQ22 (DQ06)	DQ22	DQ14 (DQ04)	DQ30	DQ6 (DQ08)
DQ7	DQ31 (DQ09)	DQ15	DQ23 (DQ07)	DQ23	DQ15 (DQ05)	DQ31	DQ7 (DQ09)
DBI0	DBI3 (DB04)	DBI1	DBI2 (DB06)	DBI2	DBI1 (DB06)	DBI3	DBI0 (DB07)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)
GDDR5 CLK Mapping							
WCK01	WCK23 (WCK04)			WCK23	WCK01 (WCK07)		
WCK01#	WCK23# (WCK05)			WCK23#	WCK01# (WCK07#)		
CK	CK						
CK#	CK#						
Others							
MF	MF	SEN	SEN				
ZQ	ZQ	RESET#	RESET#				

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

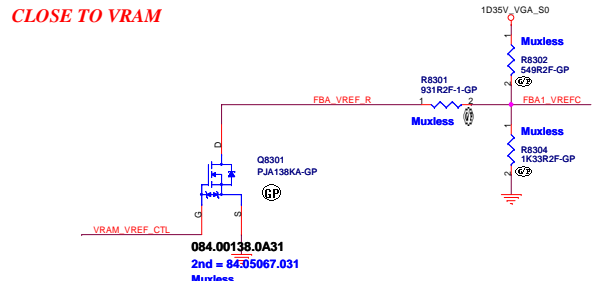
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

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Title				
		<b>VRAM 3,4 (2/4)</b>		
Size	Document Number			Rev
Custon		<b>Buzz_KBL</b>		<b>2</b>
Date	PROB, JUN 07, 2017	Sheet	B2	of 16A

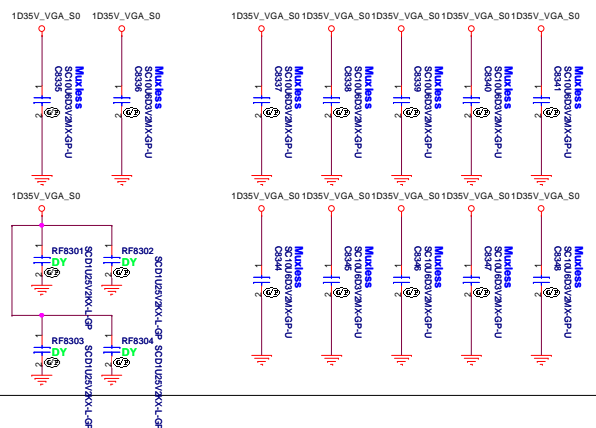
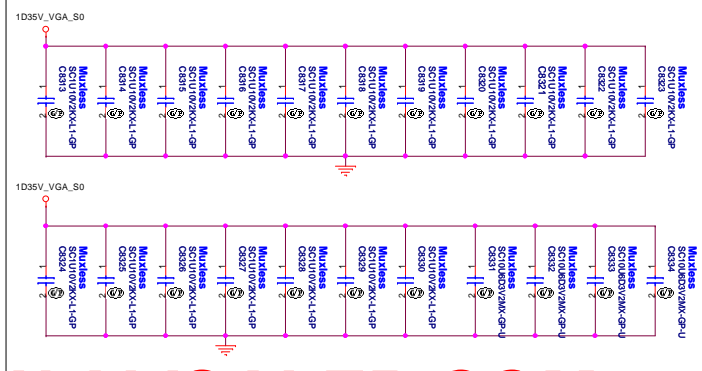


# FOR VRAM1/ VRAM2

CLOSE TO VRAM

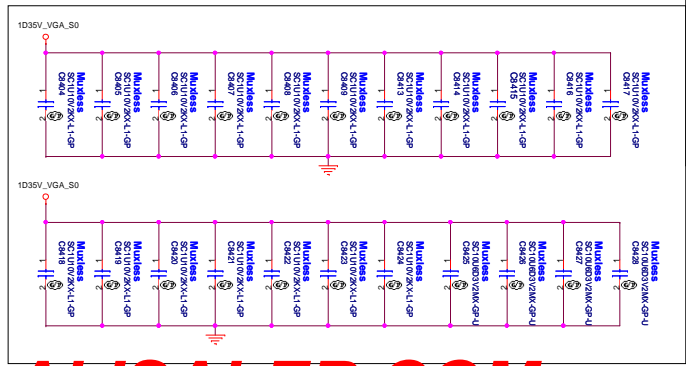
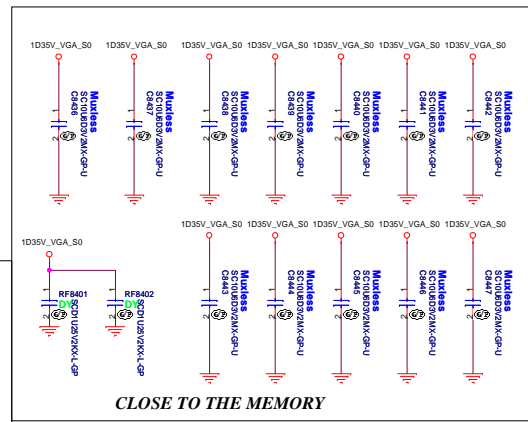
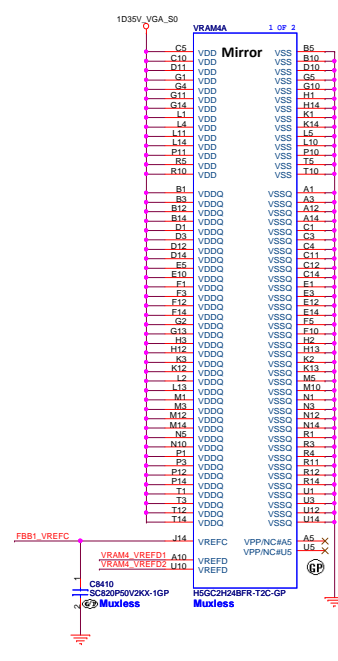


## FOR VRAM1/ VRAM2



## CLOSE TO THE MEMORY

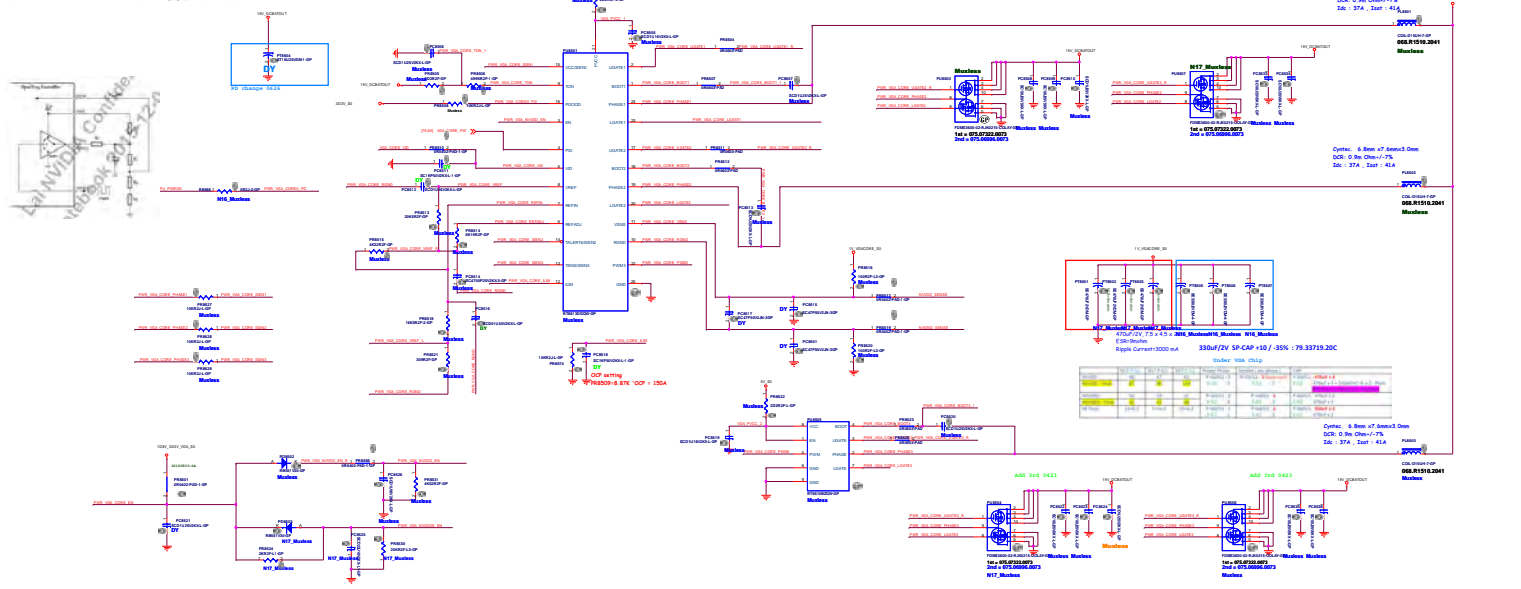
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21F, 88, Sec.1, Han Tai Wu Rd., Heichin, Taipei Hsin 221, Taiwan, R.O.C.		
Title		
VRAM_5,6 (3/4)		
Size		
Document Number		
Buzz_KBL		
Rev		
2		
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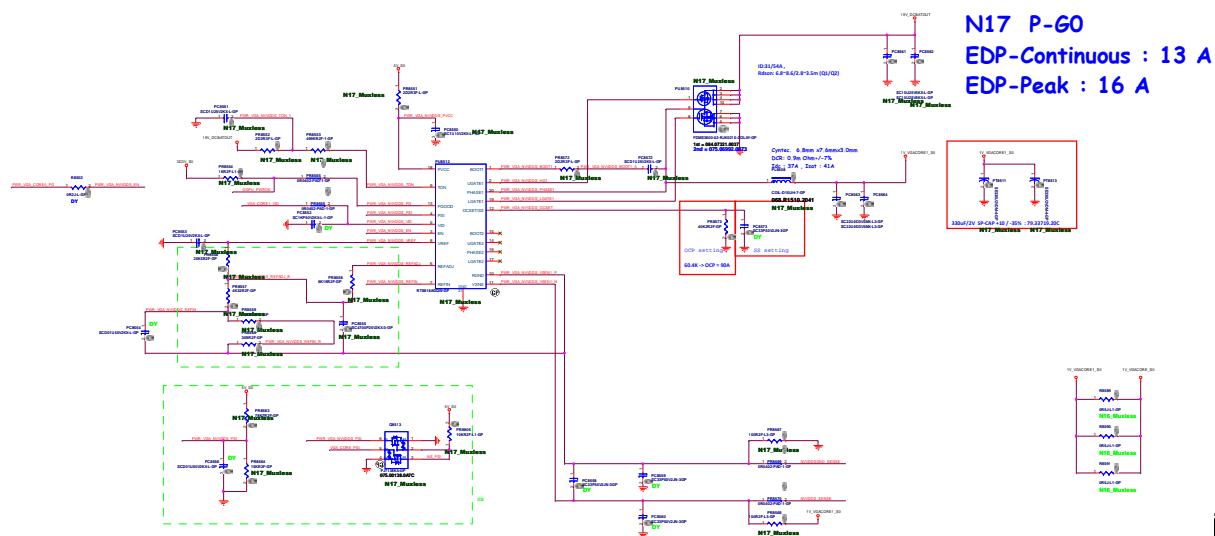
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Size	Document Number	Rev	
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Table 7-8 PWM-VID Spec and Component Values

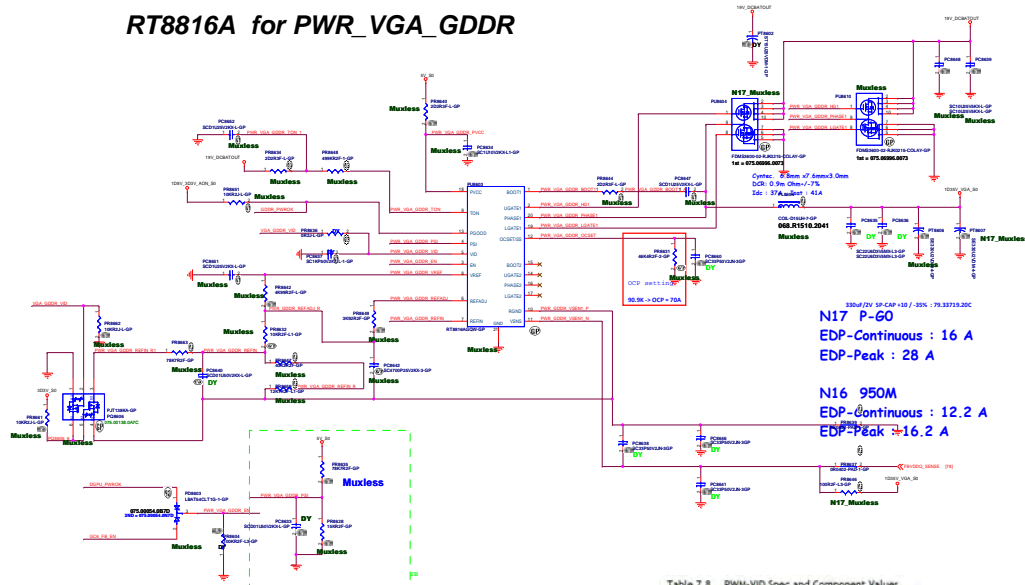
PWM-VID Specification			
	Unit	Config	
Number of Voltage Levels (N)	Level	160	
PWM Frequency (F <sub>sw</sub> )	kHz	8.75	
PWM Minimum Pulse Width (T <sub>min</sub> )	ns	9.26	
VID Transient Time (T <sub>t</sub> )	ns	>150	
Component Value			
R1 (1k)	Ω	8.19	
R2 (1k)	Ω	20.3	
R3 (1k)	Ω	4.32	
R4 (1k)	Ω	16.5	
R5 (1k)	Ω	9.26	
C	μF	1.5	



## RT8816A For NVVDDS



## RT8816A for PWR\_VGA\_GDDR



N17 P-60  
EDP-Continuous : 16 A  
EDP-Peak : 28 A

N16 950M  
EDP-Continuous : 12.2 A  
EDP-Peak : 16.2 A

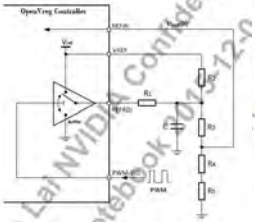
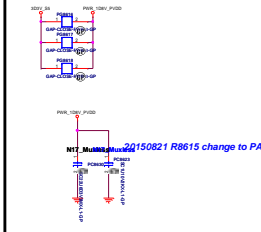


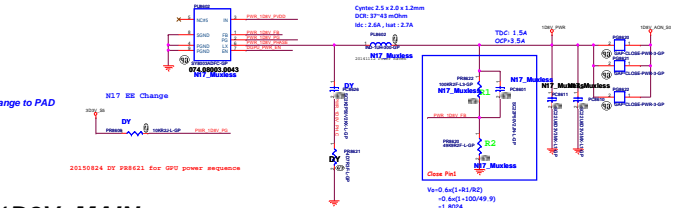
Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
Number of Voltage Levels II	Level	160
PWM Frequency F <sub>sw</sub>	MHz	6.75
PWM Minimum Pulse Width T <sub>pw</sub>	ns	9.26
VID Transient Time T <sub>VID</sub>	ns	~1000
Component Value		
R1 (1%)	R2	6.19
R2 (1%)	R3	20.5
R3 (1%)	R4	4.32
R4 (1%)	R5	14.5
R5 (1%)	R6	0.497
C	μF	

VGA\_CORE&1D05V\_VGA\_S0 Discharge Circuit  
3D3V\_S5 to 1D8V\_AON\_S0



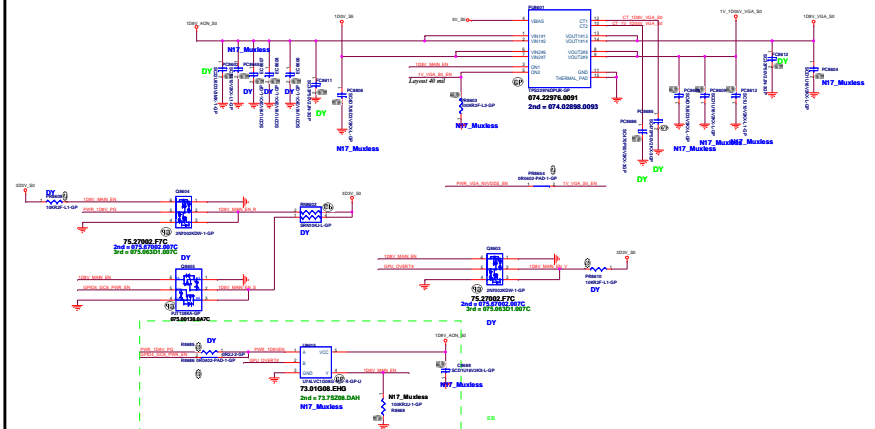
## SYW232 for 1D8V\_AON



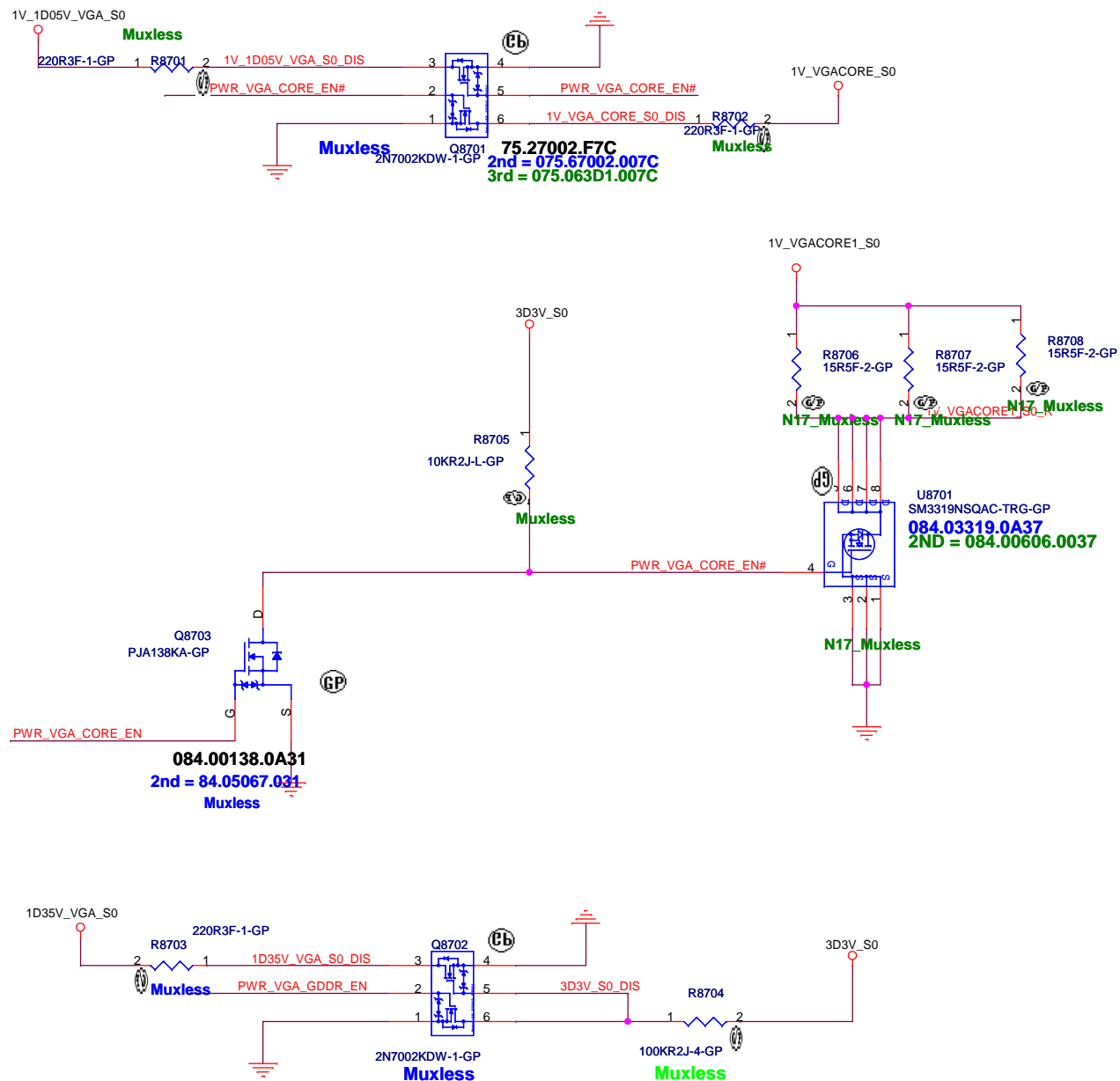
SYW232 for 1D05V  
Enable=1.5V  
Disable=0.4V

## SYW232 for 1D8V\_MAIN

N17 change to ANPEC AP13526/B



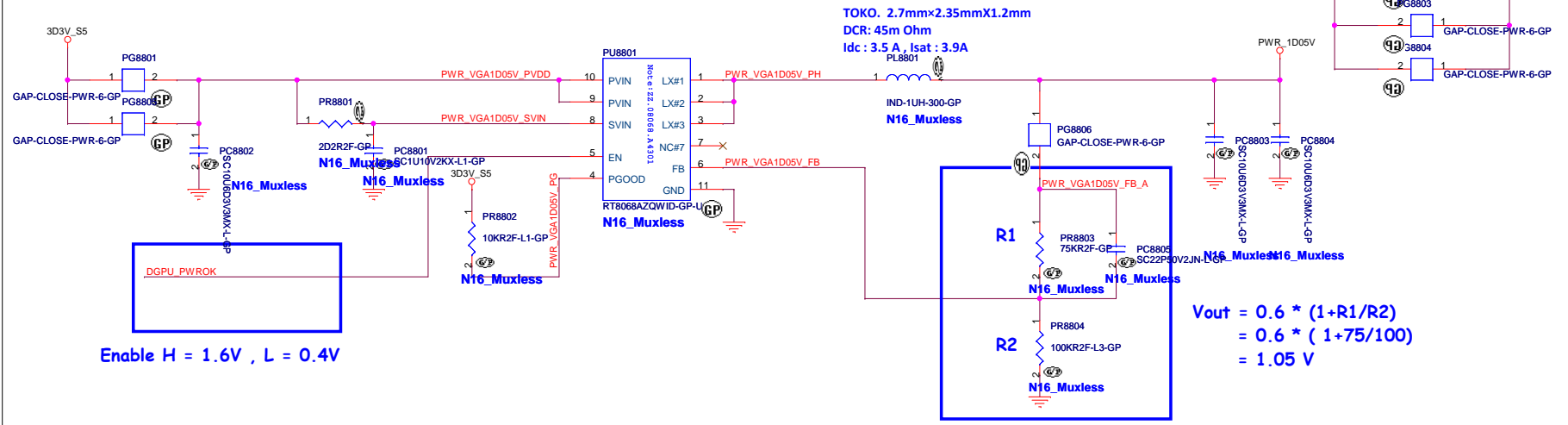
## APL3526QB for 1V\_VGA\_S0



[6] DGPU\_PWR\_EN# >>>  
[24,76,85,86] DGPU\_PWROK >>>  
[6,79,86] GC6\_FB\_EN <<<  
[79,86] GPIO4\_GC6\_PWR\_EN >>>  
[86] DGPU\_PWR\_EN >>>

# 1D05V\_VGA\_S0

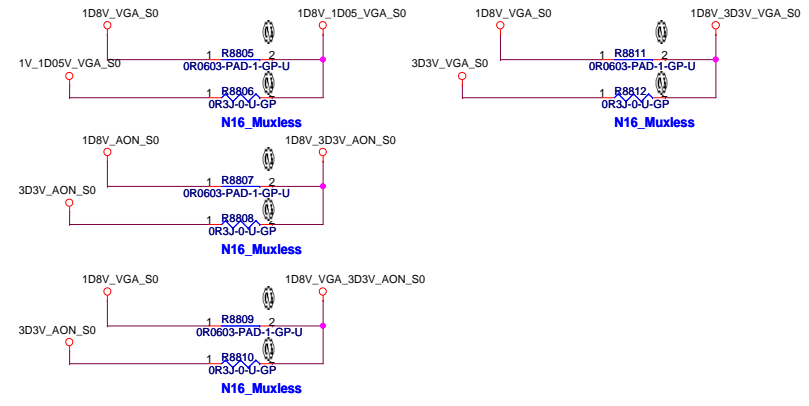
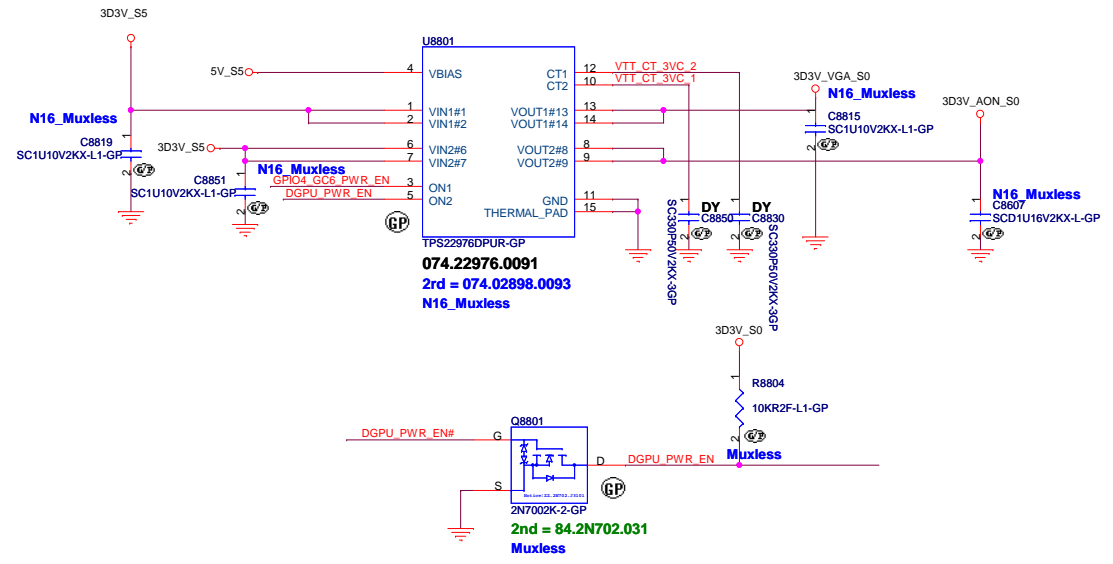
Freq = 1M Hz



Enable H = 1.6V , L = 0.4V

$$V_{out} = 0.6 * (1 + R1/R2) = 0.6 * (1 + 75/100) = 1.05V$$

## 3D3V\_S5 to 3D3V\_VGA\_S0



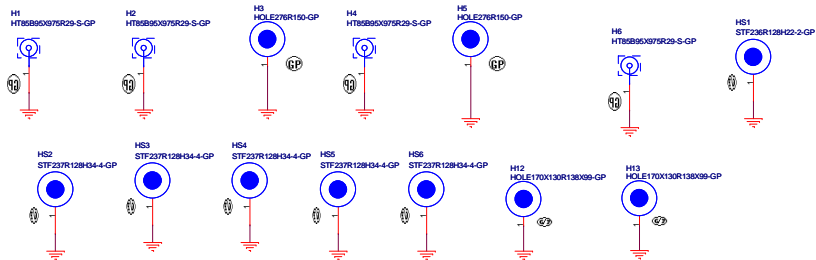
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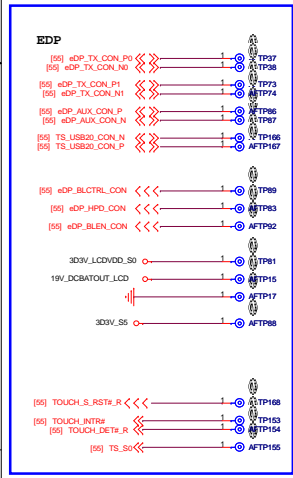
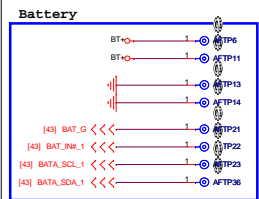
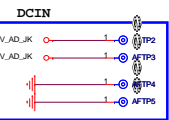
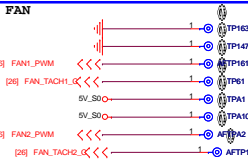
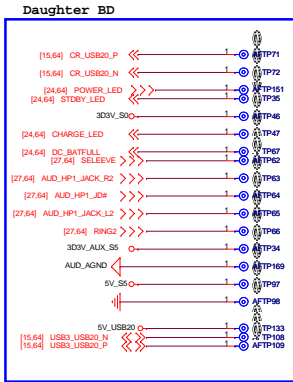
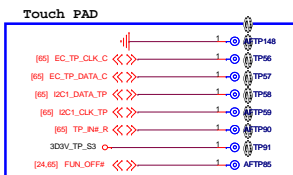
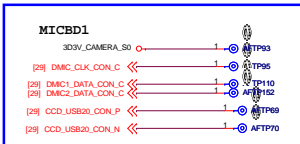
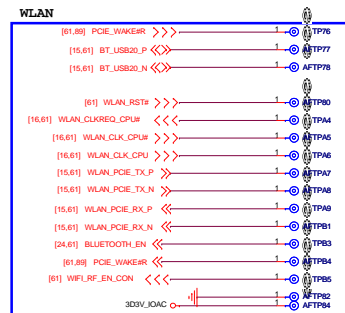
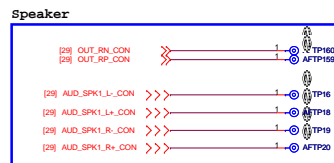
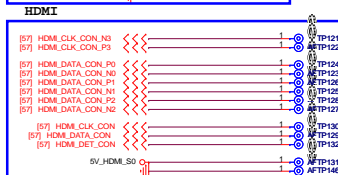
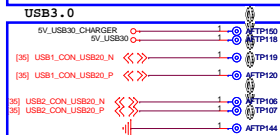
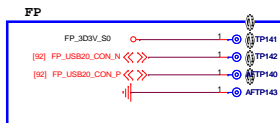
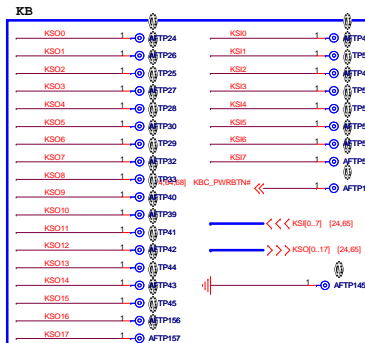
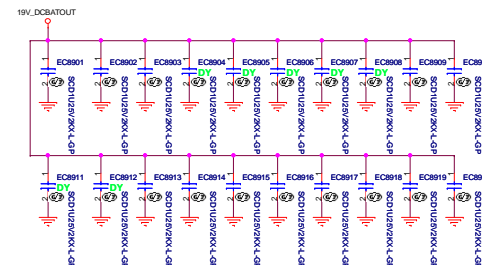
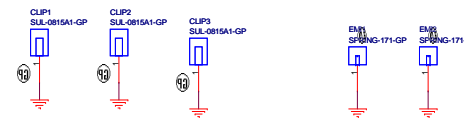
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Check test point



Top side



EMI Solution

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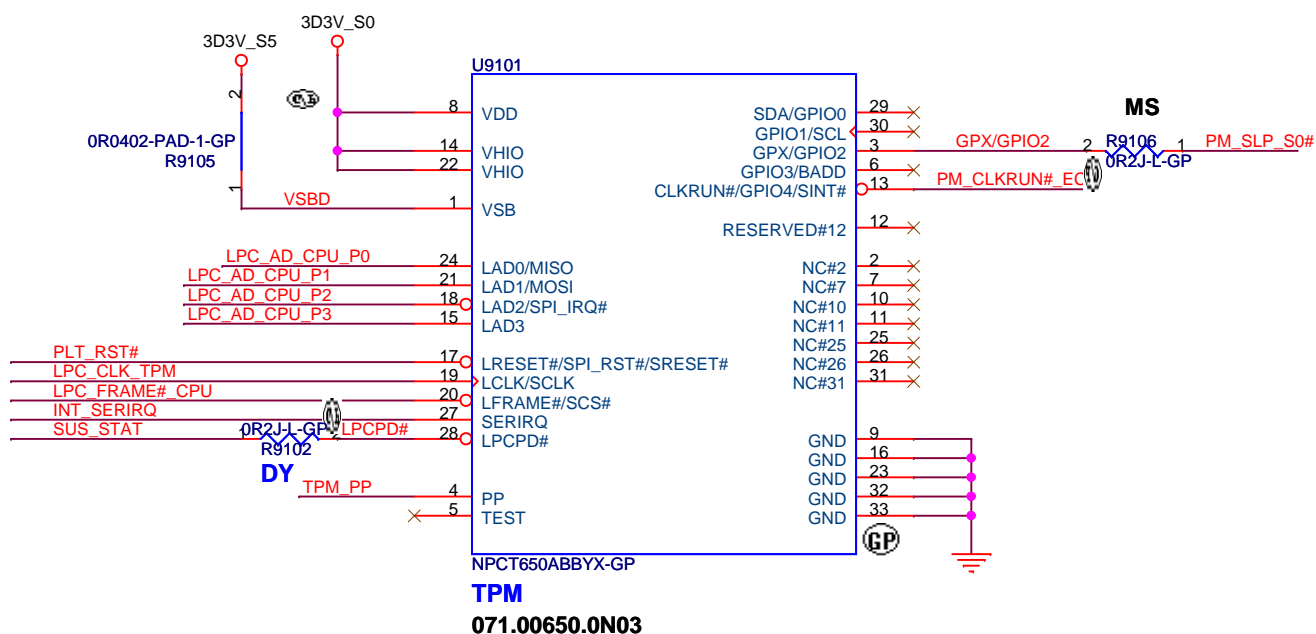
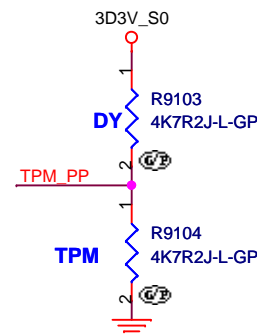
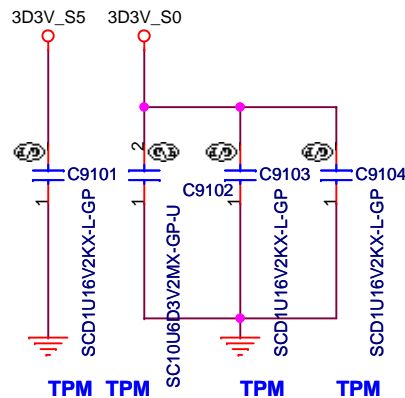
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 [18,24,68] LPC\_AD\_CPU\_P1  
 [18,24,68] LPC\_AD\_CPU\_P2  
 [18,24,68] LPC\_AD\_CPU\_P3  
 [18] LPC\_CLK\_TPM  
 [18,24,68] LPC\_FRAME#\_CPU  
 [20,24,61,62,68,79,89] PLT\_RST#  
 [18,24,68] INT\_SERIRQ  
 [18,24] PM\_CLKRUN#\_EC  
 [18] SUS\_STAT  
 [20,40,60] PM\_SLP\_S0#



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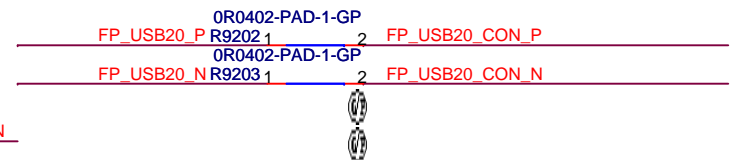
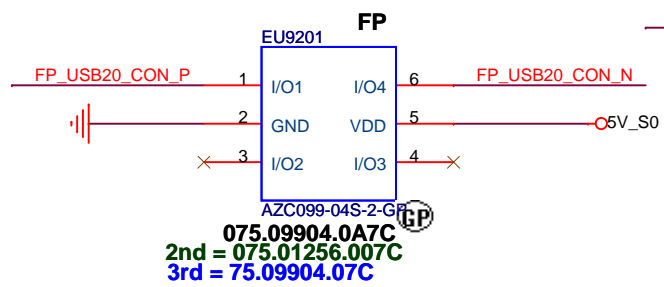
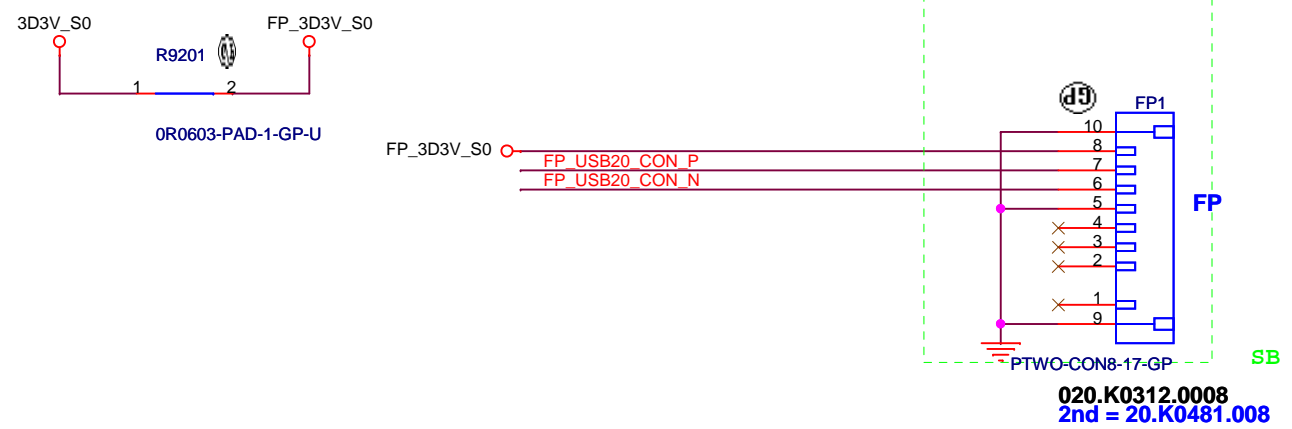
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[15] FP\_USB20\_N << >> \_\_\_\_\_  
[15] FP\_USB20\_P << >> \_\_\_\_\_  
  
[89] FP\_USB20\_CON << >> \_\_\_\_\_  
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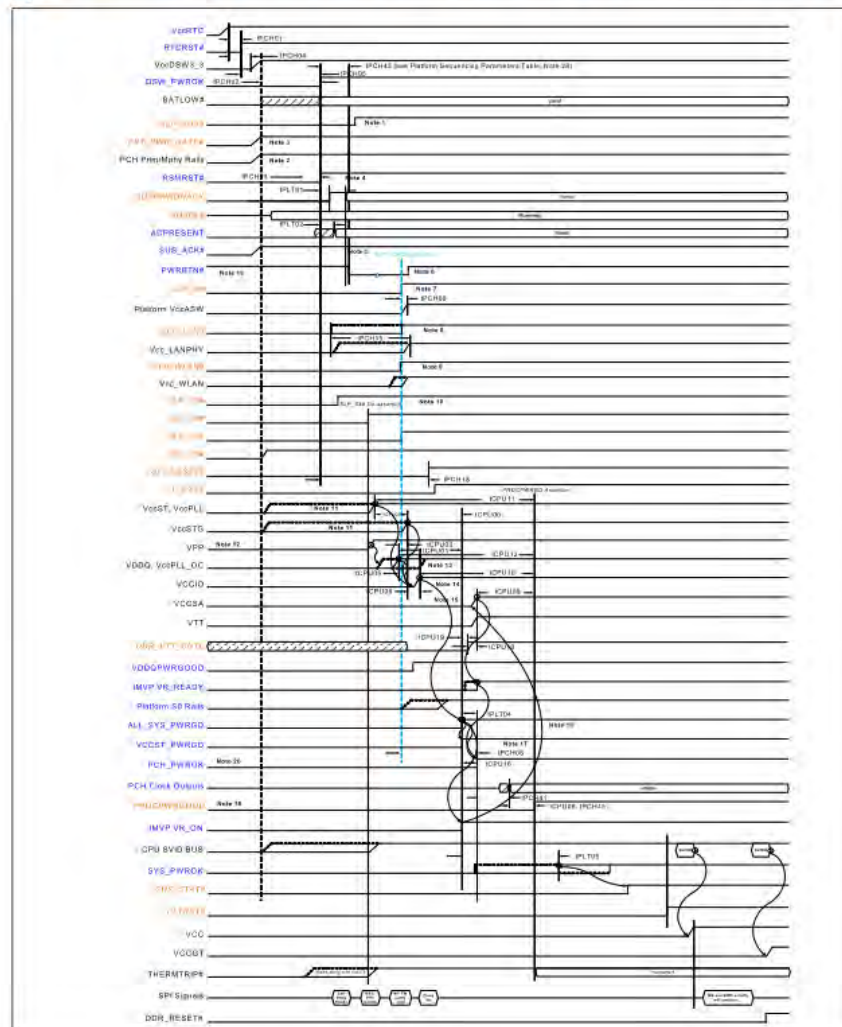
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**Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)**



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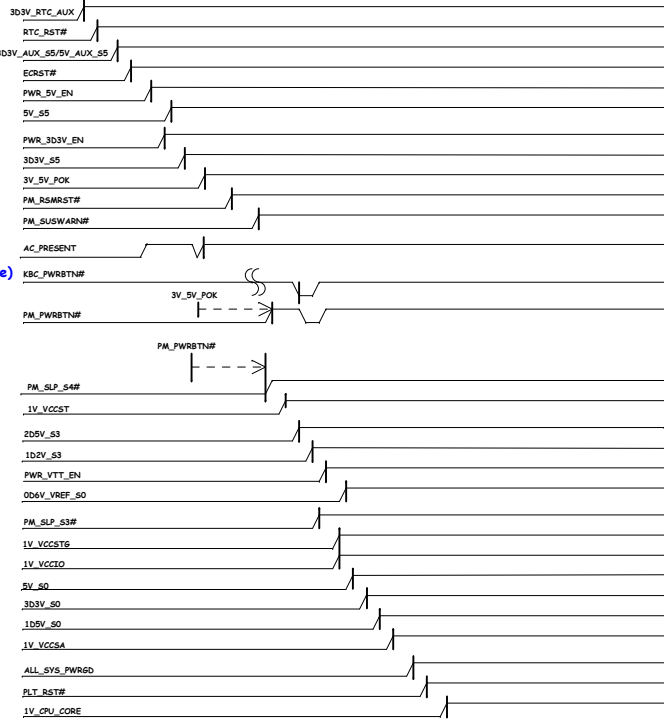
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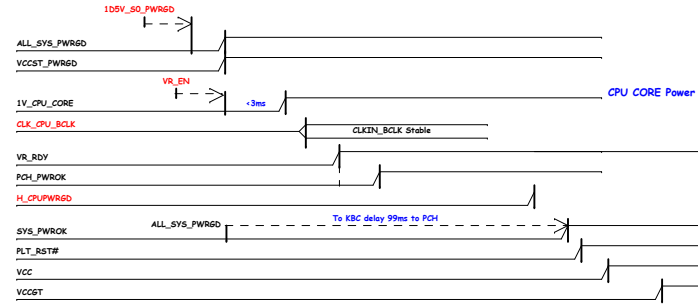
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## Intel-Power Up Sequence

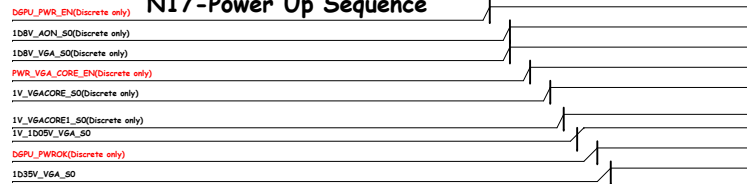
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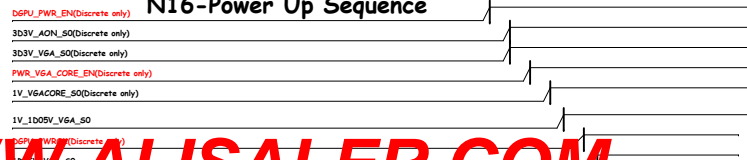
(AC mode) (DC mode)



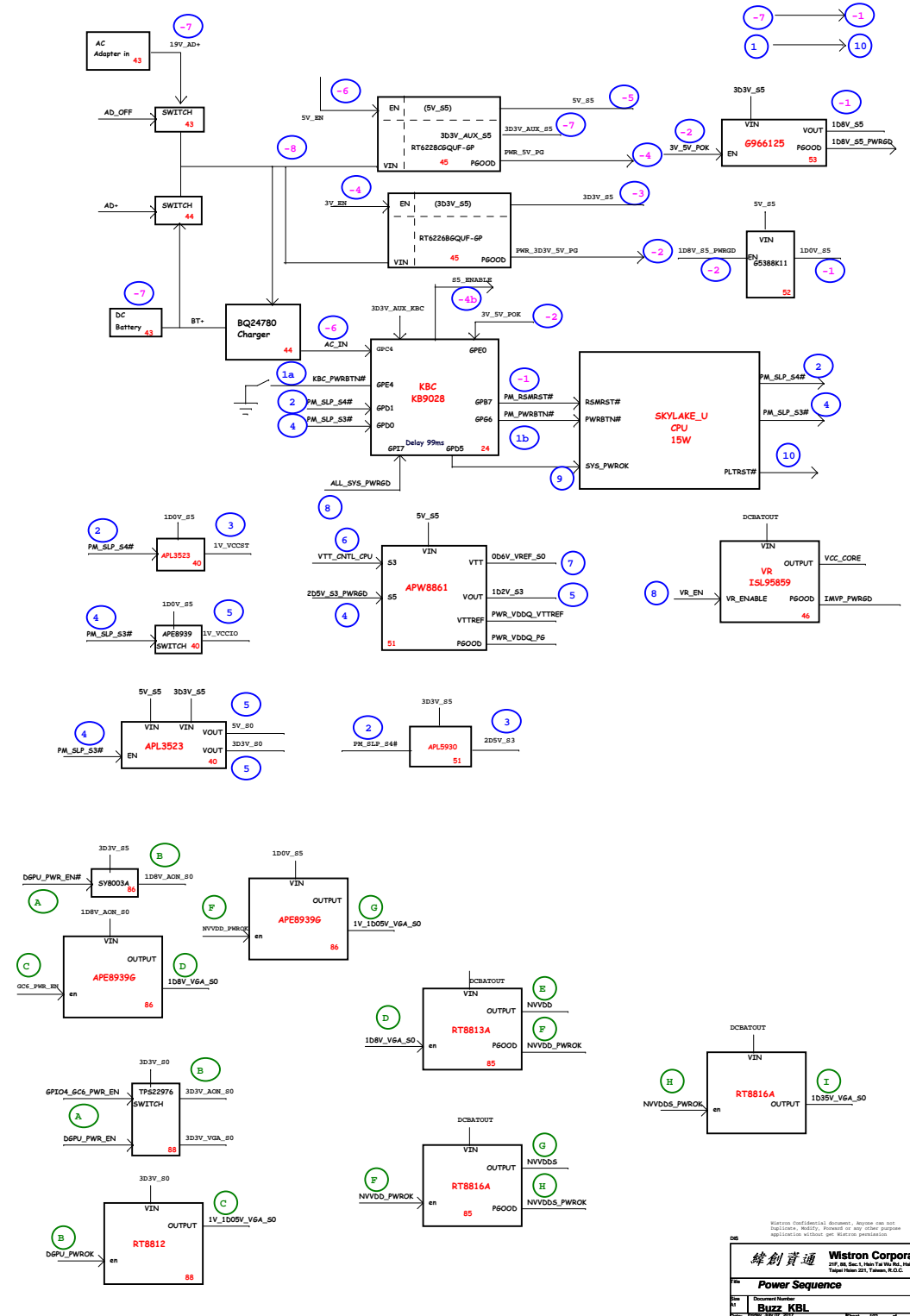
## N17-Power Up Sequence

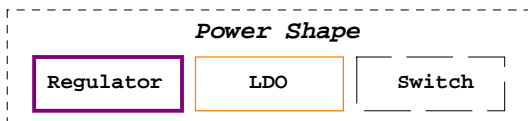
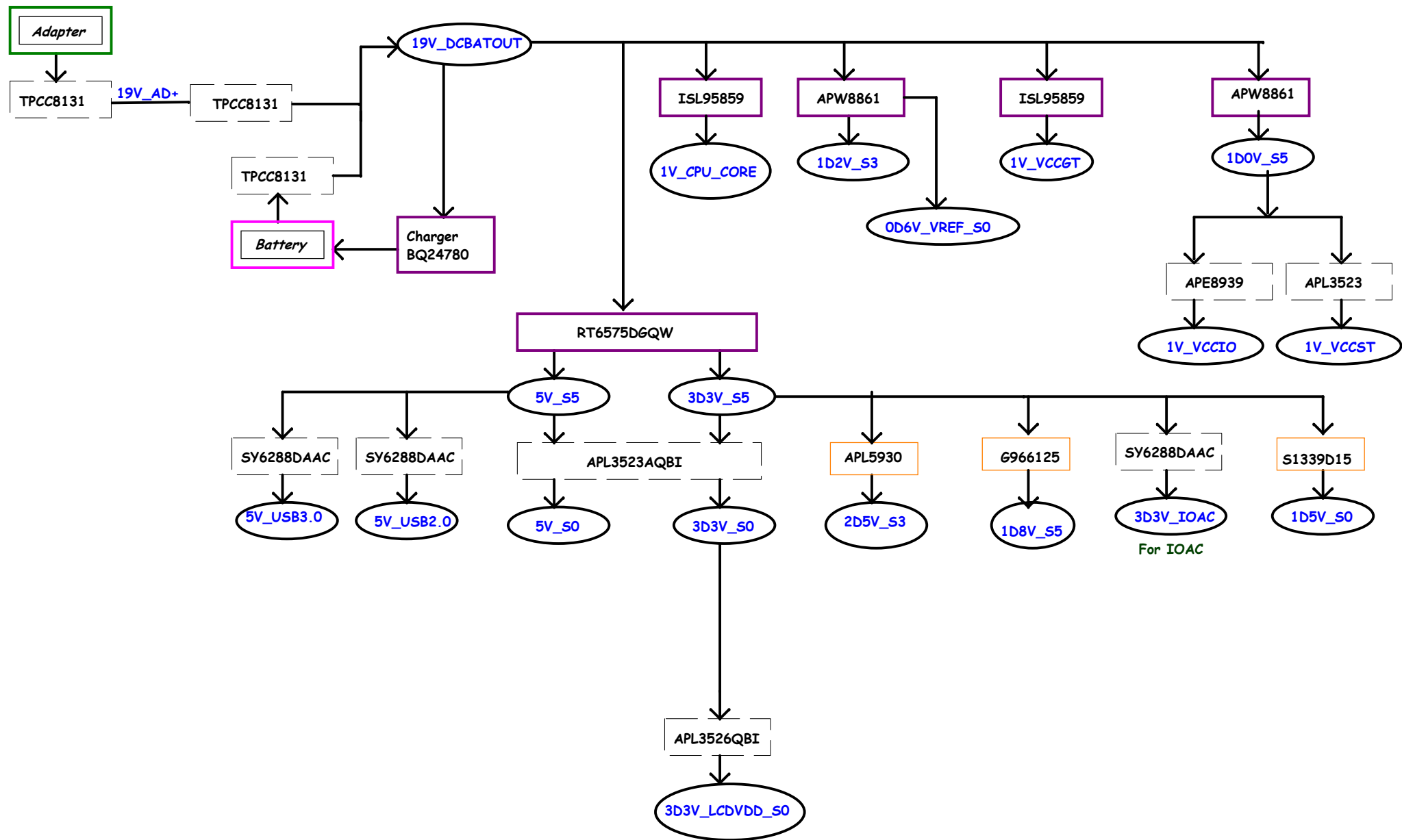


## N16-Power Up Sequence

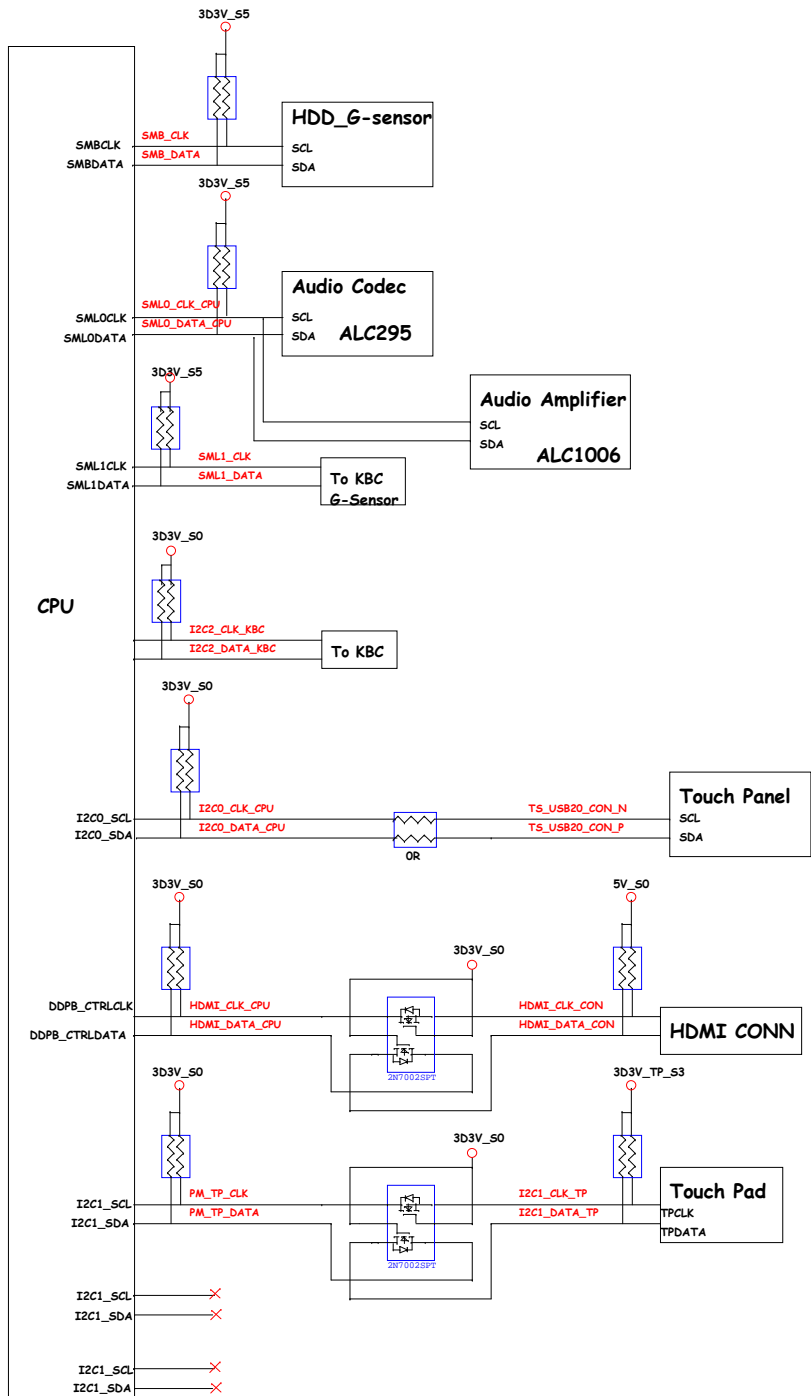


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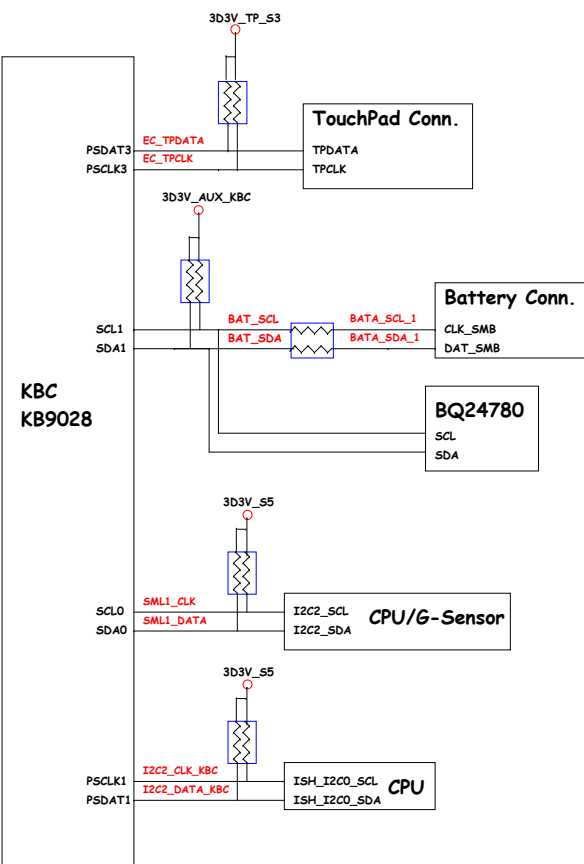




PCH SMBus/I2C Block Diagram



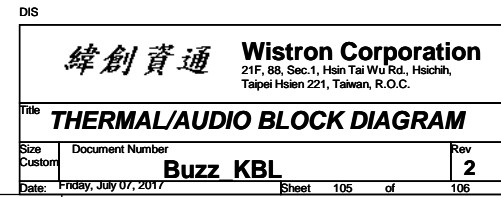
KBC SMBus/I2C Block Diagram



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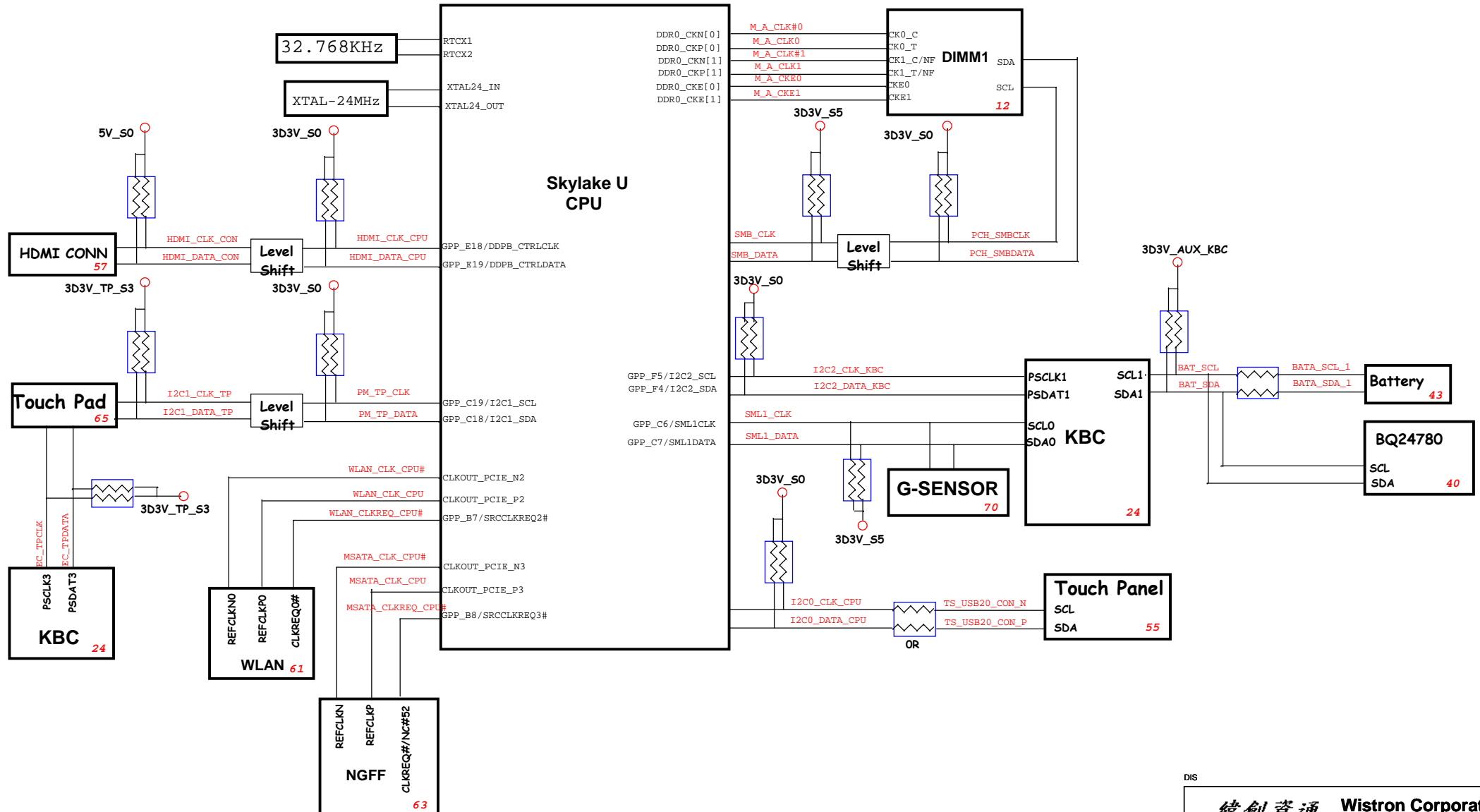


The diagram illustrates the ALC295 codec's connections to three external components: Speaker, HP Out, and DMIC.

- Speaker Connections:**
  - SPK-OUT-L- connects to AUD\_SPK1\_R\_L-
  - SPK-OUT-L+ connects to AUD\_SPK1\_R\_L+
  - SPK-OUT-R- connects to AUD\_SPK1\_R\_R-
  - SPK-OUT-R+ connects to AUD\_SPK1\_R\_R+
- HP Out Connections:**
  - HPOUT-L\_PORT-I-L connects to AUD\_HP1\_JACK\_L2
  - HPOUT-R\_PORT-I-R connects to AUD\_HP1\_JACK\_R2
  - MIC2-L\_PORT-F-L/RING connects to RING2
  - MIC2-R\_PORT-F-R/SLEEVE connects to SELEEVE
  - SENSE\_A connects to the HP Out block via a resistor.
- DMIC Connections:**
  - DMIC-CLK connects to the DMIC block.
  - DMIC-DATA1 connects to the DMIC block.
  - DMIC-DATA2 connects to the DMIC block.



# CLOCK BLOCK DIAGRAM



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